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TYPE 2B PROCESSOR COMPLEX SYSTEM MONITOR DESCRIPTION AND OPERATION

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1. GENERAL

1.01 This section provides description and operation information on the system monitor used in the Type 2B Processor Complex.

2. FUNCTION

2.01 The system monitor scans software activity and certain internal functions in the central processor complex for diagnostic purposes. The system monitor is activated ~~buy~~ by user commands.

2.02 The two primary functions of the system monitor are to trace instruction flow within a Central Processor Unit (CPU) by monitoring addresses of instructions being executed, and to trace data flow for a selected system bus function by monitoring the system command bus and system response bus along with status information from an active CPU.

2.03 Secondary functions of the system monitor include tracing changes to the general registers (GR0 through GR7) during instruction traces and performing a self-test upon command.

2.04 Modules may be installed in the system monitor to provide an X-ray test set subsystem. Printed wiring card slots are provided for the X-ray control card, the power supply, and up to 4K-(K =1,024)-by-48-bits of X-ray Read Only Memory Simulator (ROMSIM). The system monitor control program contains the necessary software driver for loading the ROMSIM, with microdiagnostics from the magnetic data cartridge to exercise a CPU.

2.05 The primary function of the X-ray test set subsystem is to execute microdiagnostics by using a CPU during system start-up. Microdiagnostics can be used to establish confidence in the CPU, the memory system, the system buses, and certain Input/Output (I/O) devices before loading macrolevel software via the system magnetic tape facility.

3. FUNCTIONAL DESCRIPTION

3.01 The system monitor is divided into four functional sections: the monitor control, the system interface, the buffer memory, and the X-ray subsystem.

Monitor Control

3.02 The monitor control section consists of the following elements (Figure 1):

(a) Microprocessor card (FB-15817).

(b) Serial device controller card (FB-15621).

(c) Modem card (FB-15092), optional.

(d) Cartridge tape system (FB-20697, FB-20725, and FD-5000-BR).

(e) Program memory card (FB-20723).

(f) Test panel interface card (FB-20712).

3.03 Microprocessor Card. The microprocessor used is the FB-15817 card, which contains an Intel 8080 microprocessor chip, Transistor-Transistor Logic (TTL) interface logic, the CPU clock circuit, 512-word-by-8-bit Read-Only Memory (ROM), 8-level priority interrupt structure, and various status and control signals.

3.04 Serial Device Controller Card. The serial device controller card (FB-15621) consists of a Universal Asynchronous Receiver/Transistor (UART), a clock circuit, and interface circuitry. Parallel inputs and outputs are compatible with the 8080 microprocessor address and data buses. Serial inputs and outputs are compatible with either Electronic Industries Association (EIA) RSA232C or 20-mA loop interfaces and are connected to either a local terminal or modem for operation with a remotely located terminal. Strapping options are provided for selecting various baud rates and word characteristics.

3.05 Modem Card. The modem card (FB-15092) is a 300-baud, FSK, answer-only card that is operationally compatible with Bell 103F-type data sets. Connection from the modem to the telephone line is via a commercially available

acoustic coupler and a standard telephone subset. Remote operation using the modem is an optional feature of the system monitor.

3.05 Cartridge Tape System. The cartridge tape system consists of a digital magnetic tape cartridge drive (FD-5000-BR), cartridge read control interface (FB-20697), and cartridge write control interface (FB-20725). The cartridge tape system is used for storage of the monitor control programs, for storage of ROMSIM programs to be executed by X-ray tests, and for software development of these programs.

3.06 Program Memory. The program memory consists of two 8K-word-by-8-bit static Random Access Memory (RAM) cards (FB-20723), giving a total of 16K words of memory for storing the system monitor control program.

3.07 Test Panel Interface Card. The test panel interface card (FB-20712) allows an operator to directly control the 8080 microprocessor by using a maintenance test panel (HS851111).

System Interface

3.08 The system interface section consists of the following elements (Figure 2):

(a) System Monitor Interface (SMI) bus receiver card No. 1 (FB-15668).

(b) SMI bus receiver card No. 2 (FB-15672).

(c) Bus receiver/pipeline card (FB-15665).

(d) Address matcher card (FB-15007) and data matcher card (FB-15008).

(e) Trace setup and control card (FB-15667).

3.09 SMI Bus Receiver Card No. 1. This bus receiver (FB-15668) receives general register data and control information from the Central Processor (CP) complex via the SMI bus. This information is buffered and presented to the trace data multiplexer (MUX) for writing into the trace buffer memory.

3.10 The SMI bus receiver No. 1 also receives system bus control information from the SMI bus receiver No. 2, and uses this information to schedule when various bus operations should be examined and saved in trace buffer memory.

3.11 The SMI bus receiver No. 1 is further responsible for receiving the system clock and distributing it to various modules within the system monitor.

3.12 SMI Bus Receiver No. 2. This bus receiver (FB-15672) receives the next execute program counter, program counter control, bus control, and other miscellaneous control information for the monitored CP complex. The bus control information is passed to SMI bus receiver No. 1, the miscellaneous control is buffered and presented to other cards via the backplane, and the program counter information is used to form next, current, and previous Instruction Address Registers (IAR).

3.13 Bus Receiver/Pipeline Card. The bus receiver/pipeline cards (FB-15665) provide termination resistors and receivers for each copy of the system command bus and system response bus from the common control system. Either or both copies of each bus may be driven onto an internal command bus and response bus through open-collector drivers to the pipeline registers.

NOTE: The pipeline registers hold system bus data for up to five system clock cycles to allow command bus data to be associated with appropriate response bus data before being written into the trace buffer memory.

3.14 Address and Data Matcher Cards. The address matcher (FB-15007) and data matcher (FB-15008) cards select the appropriate addresses and masked data words to be used as trace start, stop, or qualification events. Address information is selected from either the address of the current instruction being executed by the monitored CPU, or from a read/write address extracted from information on the system command bus.

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[illegible]

[illegible]

[illegible]

3.20 Trace Data Multiplexer Card. The trace data multiplexer card (FB-15666) selects the set of data to be written into the buffer memory array during instruction or data traces. During instruction traces, the previous instruction address, current instruction addresses, and any changes to general registers GR0 through GR7 are written; during data traces, the address of the current instruction being executed is saved along with the read/write address and read/wirte data for the selected bus function.

3.21 The buffer memory is designed to operate at a 200 ns cycle time to allow it to gather information during each system bus time slot with a minimum amount of buffering.

X-Ray Subsystem

3.22 The X-ray subsystem of the system monitor consists of three X-ray ROMSIM cards (FB-15673), one X-ray control card (FB-15674), one X-ray buffer card (FB-15675), and a +5 volt converter module card (FB-15003). The X-ray ROMSIM, X-ray control, and +5 volt module cards physically reside within one of the system monitor card files, while the X-ray buffer card is located at the CPU-under-test (Figure 3).

3.23 X-ray ROMSIM Card. Each X-ray ROMSIM card (FB-15673) contains a 1K-word-by-16-bit high-speed RAM memory array. Three ROMSIM cards together form a 1K-by-48-bit array that is used to expand or replace the CP on-board ROM during microinstruction execution.

NOTE: Additional connectors are wired to accept three additional ROMSIM cards for a maximum array size of 4K-by-48-bit. External cooling and power are required for array sizes other than the basic 1K-by-48 bits.

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3.~~23~~ 24 X-ray Control Card. The X-ray control card (FB-15674) contains the necessary address interface logic to load the X-ray ROMSIM array from the magnetic cartridge reader or to access data words based upon the CP-under-test microaddress lines. The X-ray control card also provides microaddress information that may be saved instead of macroaddress information during microdiagnostic execution.

3.~~24~~ 25 X-ray Buffer Card. The X-ray buffer card (FB-15675) contains drivers, receivers, and terminators to provide an interface between the X-ray ROMSIM and CP-under-test. Because of the rapid access time required of the X-ray ROMSIM, the physical cable lengths between the system monitor and CP-under-test for X-ray functions must be limited to less than or equal to 5 feet.

3.~~25~~ 26 The X-ray buffer card also contains a comparator with switches that can be used to select a microaddress oscilloscope synchronization test point.

4. OPERATIONAL CHARACTERISTICS

General Operation

4.01 The system monitor is activated by the user via commands, trace parameters, and other data entered at the terminal keyboard. The monitor program interprets the data and accordingly selects: the physical buses and bus functions to monitor; the start and stop events to be used; appropriate address, data, and data mask information; and the type of trace to be performed.

4.02 When the selected start event occurs, the capturing of information from the selected bus operations begins. Trace data is assembled by the system monitor from the system buses, inputted to the system interface cards, and then loaded into the buffer memory.

4.03 Depending on the start and stop events chosen, the user may elect to have all events between the start and stop events captured in the buffer memory, or to capture ~~on~~ only specified events.

4.04 When the selected stop event occurs, buffer loading is terminated. The monitor program reads the trace buffer memory, formats the data, and outputs the data via the terminal printer.

4.05 The system monitor cannot statically dump system data because it does not have direct access to the memory complex.

4.06 Via keyboard entries, the operator can change trace parameters, terminate a trace, terminate the trace dump, or selectively dump specific areas of the trace buffer.

4.07 The system monitor does not provide conditionality or masking of general register data.

4.08 The X-ray subsystem, if installed, may be activated, after the basic system monitor trace parameters are entered. Execution of X-ray microdiagnostics is discussed in part 6.

Types of Terminal Input

4.09 The user communicates with the system monitor by entering input messages on the system keyboard terminal. The system monitor control program recognizes three types of keyboard-entered data: monitor commands; trace parameters; and control characters.

Monitor Commands

4.10 Monitor commands are initiated by the user to alert or control the main scan portions of the system monitor program.

4.11 The following is a list of monitor commands recognized by the monitor program:

(a) TRACE - Indicates that a trace operation setup is required.

(b) EDIT - Indicates that an edit feature, which will affect the trace buffer printout, is required.

(c) HITS - Requests printing of the number of HITS (trace events) stored in the trace buffer after the start event was received.

(d) STOP - Reception of a stop event is simulated by the operational program and the printing of the trace buffer data will begin.

(e) GO - Restart printing of trace buffer data.

(f) RESTART - Re-enable system monitor control logic to perform a trace operation by using the data previously entered.

(g) DUMP - Request to print unique or range of trace buffer locations.

(h) MODIFY X - Request to modify TRACE prompter data where X defines the line to be modified.

(i) BTEST N - Request to execute a system monitor self-test.

(j) LOAD - Request to load the operational program.

(k) XRAY - Request to enter X-ray setup mode.

System Monitor Trace Parameters

4.12 ~~Input~~ trace parameters allow the user to structure the trace operation as desired, by selecting: the physical buses and bus functions to be monitored; the starting and stopping events to be used; the type of trace to be performed; the mode in which the trace is to be performed; and various editing options to be performed as the trace data is outputted.

4.13 Bus Selection. The user may select one of the following three bus configurations to be monitored:

(a) System command bus 0 and system response bus 0.

(b) System command bus 1 and system response bus 1.

(c) The logical-OR of system command bus 0 and system command bus 1 and the logical-OR of system response bus 0 and system response bus 1.

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The system monitor does not trace bus status responses.

4.14 Start/Stop Events. In a trace operation, the start and stop events designate when information capture in the trace buffer memory begins and when it terminates.

4.15 Possible start events are as follows:

(a) A firmware flag in the monitored system.

(b) A selected external event.

(c) A program command (keyboard input).

(d) An exact address match (with or without data match).

(e) An address within a designated range (with or without data match).

(f) An address out of a designated range (with or without data match).

4.16 For traces beginning with a non-address start event, all events between the start and stop events are captured. If ~~an address constitutes~~ the start is an address event, the user may choose to capture all trace events between the start and stop events or to capture only those events satisfying the start address and, if applicable, data parameters.

4.17 Possible stop events are as follows:

(a) A firmware flag in the monitored system.

(b) A selected external event.

(c) A program command (keyboard input).

(d) An exact address match (with or without data match).

(e) An address within a designated range (with or without data match).

(f) An address out of a designated range (with or without data match).

(g) A trace buffer overflow.

4.18 The selection of start/stop events depends on the type of trace being performed. During instruction or transfer traces, the start/stop event choices are limited to the combinations shown in Figure 4. This is because a single

set of address and data matchers is used for specifying start/stop address and data events. However, during data traces, an extra address matcher is available to allow trace events to be qualified with an exact instruction address or range of instruction addresses in addition to the read/write address and data.

4.19 Trace Types. The following types of trace operations are possible:

(a) Instruction trace (INS). As each macroinstruction is executed, its address and the address of the last instruction executed are captured. In addition, if the present instruction causes a modification to the contents of a general register (GR0 through GR7), the identities of the general register and the modified register contents are captured. The current instruction address being executed is used by the matchers for start/stop events.

(b) Transfer trace (XFER). If ~~an instruction is determined to be~~ a transfer instruction, both the address of the transfer instruction and the "transfer-to" address are captured. If the transfer instruction causes a modification to the contents of a general register ~~(GR0-7)~~ after a FETCH bus command has been issued, the identities of the general register and the modified register contents are captured. The "transfer-to" address is used by the matchers for start/stop events.

(c) Data traces. When a read and/or write operation is performed, the program address of the current macroinstruction being executed, the logical read/write address and the read/write data are captured in the trace buffer. There are five kinds of data traces.

(1) Instruction Store (IS) data trace. This trace is performed for a READ or WRITE system bus operation that is mapped to an instruction store portion of memory. The FETCH operations from the IS are not captured.

(2) Process Store (PS) data trace. This trace is performed when READ or WRITE bus operations are mapped to process store portions of memory.

(3) Memory data trace (MEM). This trace is for any system bus operations to or from the memory except pipeline fetches.

(4) Peripheral Controller (PC) data traces. This trace is for a system bus operation that accesses the PC complex.

(5) Direct Memory Access (DMA) data trace. This trace is for a system bus operation that is a DMA READ or WRITE to memory. In this case, the address of the previous macroinstruction executed is captured in the trace buffer instead of the current instruction.

(d) Command trace (CMD). All system command bus operations, including pipeline fetches and memory refresh operations, are traced to give a complete picture of bus activity. The logical address is also traced, if available, along with the actual command. The type of bus operation being performed can be determined from a five-bit bus operation code saved in the trace buffer with each trace event. The possible bus operation codes are shown in Figure 5.

4.20 Trace Modes. There are two trace modes: progressive and regressive.

4.21 A progressive trace captures up to 2,048 events following the selected start event. Buffer loading is terminated and printing begun either when the stop event occurs or when the trace buffer overflow indicator is activated, depending on which occurs first. Data is printed on a First-In-First-Out (FIFO) basis, thereby showing the progress of the program flow after a selected start event.

4.22 A regressive (history) trace, also captures up to 2,048 events. However, if the trace buffer becomes full, the oldest data is replaced with the most current data. Thus, buffer loading is continuous and is only terminated when

the selected stop event occurs. Data is then printed out on a Last-In-First-Out (LIFO) basis, giving a history of the last 2,048 events preceding the stop event.

4.23 Edit Options. The edit parameters are software, post-processing options to selectively print out only portions of the trace buffer after a trace is completed. Edit options are discussed in part 5.

Control Characters

4.24 The following characters, when entered on the keyboard terminal, are recognized by the system monitor control program as control characters:

(1) CTL-X (CAN); Abort operation and return to monitor program.

(2) CTL-B (STX); Indicates beginning of monitor command or line deletion.

(3) CTL-C (ETX); Indicates end of monitor command or response to prompter.

(4) CTL-Z (SUB); Used only after a LOAD command.

(5) $(DOLLAR SIGN); Terminal-entered character delection.

Input Message Format

4.25 Monitor Command Input Format. To activate the system monitor, the user first enters the control character CTL-B (STX) on the keyboard terminal. When the monitor program recognizes the control character, and "I*" is printed out, beginning at column 1. The user then enters the monitor command, followed by a CTL-C (ETX) control character entry to indicate the end of the command.

Example:

<STX>

I* <COMMAND> <ETX>

where: < > specifies user's input.

4.26 Prompter Response Input Format. After a monitor command is inputted, the monitor program may then generate a sequence of prompter questions. The

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prompter response consists of either hexadecimal data or one of several choices that may be indicated in the prompter question. After inputting the desired response, the user enters a CTL-C (ETX) control character to indicate the end of the response entry. Example:

'Prompter Question =' <Prompter Response> <ETX>

where: < > specifies user's input.

4.27 System monitor trace parameters are entered as prompter responses to prompter questions.

4.28 If the user's input is not acceptable because of excessive characters or no match with valid entries, the monitor program reprompts the questions and waits for a new user input.

4.29 Control Character Input Format. The following examples indicate the uses and input formats of various control characters.

4.30 Error Correction. The control character, $ (dollar sign), is used for character delection. Each "$" entered via the terminal deletes one previously entered character. Example:

4 START(ADDR,EXT,IMMED) = <IMMA$ED> <ETX>

where: < > specifies user's input.

4.31 Line Deletion. To delete a complete line of data, enter a CTL-B (STX). All data entered to the left of the control character will be deleted. Example:

4 START(ADDR,EXT,IMMED) = <IMMED> <STX> <ADDR> <ETX>

5 ETC.

where: < > specifies user's input.

4.32 Abort Function. A CTL-X (CAN) entry can be used to return control to the monitor program and abort the function currently in progress. Example:

4 START(ADDR,EXT,IMMED) = <CAN>

INPUT ABORTED

<STX>

I* <TRACE> <EXT>

ETC.

where: < > specifies user's input.

4.33 Trace Buffer Dump Stop. To halt the dumping of the trace buffer data, all that is required is the entering of a CTL-B (STX). Upon recognition of the STX, the printing of the trace buffer stops, an "I*" is printed, and the monitor program waits for a new command input.

4.34 If the STX is entered to halt the trace buffer dump while the system monitor is in the auto-restart mode, the dump is halted and the control program ~~exists~~ exits from the auto-restart mode.

5. COMMAND DESCRIPTION

NOTE: In all of the command descriptions below, < > specifies user's input.

TRACE Command

5.01 General Operation. The TRACE command activates the system monitor to perform its primary function of scanning software activity in the central processor complex. The monitor control program responds to the keyboard entry of a TRACE command by generating a sequence of prompter questions that enable the user to define the exact trace operation desired. This sequence of prompter questions and responses constitutes the setup of a trace operation. Execution follows the setup and concludes with a printout of the scanned software activity.

5.02 Relationship to other Monitor Commands. The following monitor commands, EDIT, HITS, STOP, GO, RESTART, DUMP and MODIFY X, can only be used in conjunction with the basic TRACE command. Essentially, these commands introduce variations in the progress of a trace operation (including the printout phase) that is

first defined and activated via the TRACE command. Some of these associated monitor commands may actually be entered as subordinate steps in the TRACE command setup phase. None can be used independently of a TRACE command to activate a system monitor operation.

5.03 The BTEST N command does not require prior entry of a TRACE command and may therefore be considered independent of the latter. In terms of a hierarchy of commands, BTEST N and TRACE may be thought of as at the same level. Both commands initiate trace operations for diagnostic purposes. However, the TRACE is used for scanning CPU software activity, while BTEST N traces are performed on the system monitor itself.

5.04 The LOAD command and TRACE command perform unrelated functions and are used independently of each other.

5.05 Use of the TRACE command is necessary in setting up an X-ray micro-diagnostic with the X-RAY command. The interrelationship of these two commands is discussed in part 6.

5.06 Input Format. Entry of the TRACE command, prompter responses, and pertinent control characters follows the input message format described in paragraphs 4.25 through 4.34.

5.07 Prompter Questions. Listed below in order of sequence are the prompter questions generated by the monitor program to elicit all necessary information, including trace parameters, to perform a trace operation. Important to note is that the prompter response given in one step may limit the available choices in the next step. A particular response may also lead to a branch sequence of prompter questions. For example, the prompter questions in steps (f) through (h) below are only generated following the selection of the ADDR response in step (d).

(a) Copy (0,1,B) = <Selection> <ETX>

Specifies the system bus copy to be monitored.

0 = Copy Zero

1 = Copy One

B = Both Copies (OR-ing of information)

(b) MODE (P,R) = <Selection> <ETX>

P = Progressive (FIFO)

R = Regressive (LIFO)

(c) TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = <Selection> <ETX>

IS = Instruction Store Data Trace

PS = Process Store Data Trace

PC = Peripheral Controller Data Trace

INS = Instruction (Program) Trace

XFR = Transfer Trace

MEM = Memory Trace

DMA = Direct Memory Access Trace

CMD = System Command Bus Trace

(d) READ-WRITE (R,W,B) = <Selection> <ETX>

This prompter question occurs only when a data trace (IS, PS, PC, MEM, or DMA) is specified in step (c) above.

where: R = Read Data Operation Only

W = Write Data Operation Only

B = Both Read and Write Data Operations

EXAMPLE:

3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = <IS> <ETX>

READ-WRITE (R,W,B) = <R> <ETX>

4 ETC.

(e) START (ADDR,EXT,IMMED) = <Selection> <ETX>

This step specifies the type of start event to be used.

ADDR = Address

EXT = External Level

IMMED = Immediate (System Monitor Control Program)

NOTE: Prompters (f) through (i) occur if ADDR is chosen in step (e).

If EXT is chosen, step (j) occurs directly after step (e).

(f) START ADDR = <1 to 10 Hexadecimal Characters>

This prompter occurs when ADDR is specified as the start event in step (c). The instruction address is used for instruction or transfer traces, while read/write logical addresses are used on data traces.

The start address can be specified as any one of the following:

(1) Exact address match (with or without data match), entered as one to five hexadecimal characters, right justified.

Example:

4 START(ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <YXXXX> <ETX>

where: Y = Page Number

XXXX = Effective Address

(2) Address within a designated range (with or without data match).

Entered as follows: R12345:6789A

Example:

4 START(ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <R12345:6789A> <ETX>

ETC.

where: R indicates in-range

If RW:Z, then W<Z

(3) Address outside a designated range (with or without data match).

Entered as follows: X12345:6789A

Example:

4 START(ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <X12345:6789A> <ETX>

where: X indicates out-of-range

If XW:Z, then W<Z

NOTE: Only one address/data matcher set is used for selecting start/stop events. This will allow only the following start/stop address combinations (Figure 4):

- Exact address start and exact address stop.
- Address range start and non-address stop.
- Nonaddress start and address range stop.

(g) EVENT CAPTURE (A,Q) = <Selection> <ETX>

This step occurs only if ADDR is specified in step (c). This prompter question allows the user to choose how events are to be captured after the start event occurs.

where: A = All. Every valid trace event is to be captured after the start event occurs.

Q = Qualified. Only those trace events which satisfy the START ADDR conditions for INS or XFR traces, or the START ADDR, DATA and/or MASK conditions for data traces, will be captured.

(For non-ADDR start event choices in step (c), this prompter is not issued because all valid trace events are captured after the non-address start event occurs.)

(h) DATA = <0 to 8 Hexadecimal Characters (right-justified)>

The DATA prompter occurs when ADDR is specified as the start event in step (c) and when a data trace (IS, PS, PC, DMA, or MEM) is specified in step (b). If data is entered, then conditions for a start event are Monitored Address = User-Designated Address and Monitored Data = User-Designated Data. The user can, by not specifying data and entering an ETX, force the data match circuitry to a DON'T CARE state for all 32-bit positions.

Example 1:

3TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = <IS> <ETX>

READ-WRITE (R,W,B) = <W> <ETX>

4 START (ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <12345> <ETX>

EVENT CAPTURE (A,Q) = <A> <ETX>

DATA = <01234567> <ETX>

Example 2:

3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = <IS> <ETX>

READ-WRITE (R,W,B) = <W> <ETX>

4 START (ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <12345> <ETX>

EVENT CAPTURE (A,Q) = <Q> <ETX>

DATA = <ETX>

(i) MASK = <0 to 8 Hexadecimal Characters

The MASK prompter occurs only when DATA is specified as in example 1 of step (h) above. The mask consists of 32-bit positions (same scheme as monitored system) where placing a "1" in a bit position will mark it as a DON'T CARE. If the user does not require the mask feature, he may, in step (h), simply enter an ETX without specifying data.

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Example 1:

4 START (ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <12345> <ETX>

EVENT CAPTURE (A,Q) = <A> <ETX>

DATA = <01234567> <ETX>

MASK = <0000FFFF> <ETX>

5 ETC.

Example 2:

4 START (ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <12345> <ETX>

EVENT CAPTURE (A,Q) = >Q> <ETX>

DATA = <01234567> <ETX>

MASK = <ETX>

5 ETC.

(j) EXT START (FRCOV,1,2) = <Selection> <ETX>

The EXT START prompter occurs when EXT is specified as the start event in step (c). The EXT start can be specified as any one of the following:

(1) FRCOV = Firmware Recovery

Example 1:

4 START (ADDR,EXT,IMMED) = <EXT> <ETX>

EXT START (FRCOV,1,2) = <FRCOV> <ETX>

5 ETC.

where: 1 = External Event 1. This is a strappable backplane level available in the active CF.

Example 2:

4 START (ADDR,EXT,IMMED) = <EXT> <ETX>

EXT START (ERPTL,1,2) = <1> <ETX>

5 ETC.

where: 2 = external event 2, same as external event 1.

(k) STOP (ADDR,EXT,OVFL) = <Selection> <ETX>

ADDR = Address, same options as for START.

EXT = External, same options as for START.

OVFL = Trace Buffer Overflow, will allow storage of 2,048 trace events.

NOTE: Steps (l) through (n) occur if ADDR is specified in step (k).

If EXT is specified, step (o) occurs directly after step (k).

(l) STOP ADDR = <VALUE> <ETX>

Stop Address. Same format as in step (f) for START ADDR.

(m) DATA = <VALUE> <ETX>

Stop Data. Same format as in step (h) for start data.

(n) MASK = <VALUE> <ETX>

Stop Mask. Same format as in step (i) for start mask.

(o) EXT STOP (FRCOV,1,2) = <SELECTION> <ETX>

External Stop. Same format as in step (j) for External Start.

(p) IAR = <Value> <ETX>

If a data trace (IS, PS, PC, DMA, MEM, or CMD) is selected in step (c), this prompter occurs after the START and STOP events are selected to allow the user to qualify data trace events with instruction addresses. Four types of response are allowed:

(1) No IAR address qualification. The feature is to be disabled.

Example:

```
5 STOP(ADDR,EXT,OVFL) = <OVFL> <ETX>
6 IAR = <ETX>
ETC.
```

(2) Exact IAR address. Only trace-selected data trace events for the specified IAR address. Entered as follows:

6 IAR = <12345> <ETX>

where: the entered address consists of one to five hexadecimal characters, right justified.

(3) IAR address inside a designated range. Entered as follows:

6 IAR = <R12345:6789A> <ETX>

where: R indicates in range.

If RW:Z, then W<Z

(4) IAR address outside a designated range. Entered as follows:

6 IAR = <X12345:6789A> <ETX>

where: X indicates out of range

If XW:Z, then W<Z

This prompter is not issued for instruction or transfer traces. If an attempt is made to change this prompt by using the MODIFY command with a parameter of 6 when performing an instruction or transfer trace, an error message will be outputted and the MODIFY command will be ignored.

(q) EVENTS = <Value> <ETX>

This prompter enables the user to limit the number of events that will be printed when a trace has completed and the trace dump begins. This feature is especially useful when using the auto-restart feature. Possible responses are as follows:

(1) If an ETX alone is entered in response to the EVENTS prompter, all trace events in the trace buffer will be printed when the trace dump starts.

(2) If a one- to three-digit hexadecimal number is entered, in the range 1 to 800, no more than the entered number of trace events will be printed.

Example:

5 STOP(ADDR,EXT,OVFL) = <OVFL> <ETX>

6 IAR = <ETX>

EVENTS = <7F> <ETX>

ETC.

The entry of 7F for events would limit the trace printout to 127 (decimal) events.

(r) READY (Y,N,E,X,A) = <Selection> <ETX>

The READY prompter informs the program either to setup the required system monitor hardware and begin execution of the trace operation or to idle and wait for further instructions. At this point, other monitor commands may be entered.

Y = Yes. This instructs the program to set up the system circuitry and to begin execution.

N = No. This causes the program to idle while waiting for further instructions. The system monitor circuitry is not affected.

E = EDIT. Entry of the EDIT monitor command is followed by a branch sequence of prompter questions, permitting selection of various printout options (see paragraphs 5.08 and 5.09).

X = X-RAY. Entry of the X-RAY command causes the program to enter the X-ray setup mode (see part 6 for the use of this feature).

A = Auto-restart. The auto-restart mode will start a new trace, using the previously entered setup parameters, as soon as the trace printout for the current trace is completed.

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After entry of an A, the READY question will be reprompted.

Example:

READY (Y,N,E,X,A) = <A> <ETX>

** AUTO-RESTART MODE **

READY (Y,N,E,X,A) = <Y> <ETX>

ETC.

The auto-restart mode is reset whenever the printout of the trace buffer is stopped by entering an STX.

Edit Command

5.08 The EDIT command allows selective printing of the captured trace buffer data. An EDIT command can be entered in either of two ways: by responding with an E to the READY question in step (r) of the TRACE command setup phase (example 2 below); or by entering the word EDIT as a discrete command on the keyboard terminal (example 2 below).

EXAMPLE 1:

4 START (ADDR,EXT,IMMED) = <IMMED> <EXT>

5 STOP (ADDR,EXT,OVFL) = <OVFL> <EXT>

EVENTS = <10> <ETX>

READY (Y,N,E,X,A) = <E> <EXT>

** EDIT MODE **

EDIT (L,D,A,R,N) = <Selection> <ETX>

EXAMPLE 2:

<STX>

I* <EDIT> <ETX>

EDIT MODE

EDIT (LD,D,A,R,N) = <Selection> <ETX>

ETC.

where: <> specifies user's input

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5.09 Type of Edit Features. The following prompter questions are generated after an E or EDIT is entered:

(a) EDIT (L,D,A,R,N) = <Selection> <ETX>

where: L = Loop inhibit. This is used for instruction and transfer trace operations only. This feature inhibits printing of trace events if the same address occurs five times, each time within three events of the previous time. An (*) will be printed and further printing of trace buffer data inhibited until the loop is completed.

D = Data edit. This feature selection allows printing of trace events whose READ/WRITE data (data trace) or general register data (instruction or transfer trace) is equal to a specific terminal entered data pattern.

A = Address edit. When selected, this feature will allow printing of trace events whose address, IAR or data address (data trace), or TO address (program or transfer trace), meets a specific terminal-entered address pattern. The address pattern, which the trace event must match to be printed, can specify either an exact address match, inside address range or outside address range.

R = Register edit. This feature is used for instruction- and transfer-type traces only. When selected, this will allow printing of trace events whose general register number (GR0 through GR7) is equal to a specific terminal-entered GR number.

N = None. Entering N causes any previously entered edit option to be removed.

(b) ADDR (IAR,RW) = <Selection> <ETX>

This prompter occurs only when a data trace (IS, PS, PC, MEM, DMA, or CMD) has been previously specified in step (c) of the TRACE command. This feature allows the user to select at which address (IAR - Program or RW - DATA) the program will perform the address edit.

(c) ADDR = <Value> <ETX>

The ADDR prompter specifies the address value which the operational program will use to search the trace buffer and allow printout. The ADDR prompter can be specified as an exact address or address range. When an exact address is entered, a search of the trace buffer will begin and only the trace events whose TO address (for instruction and transfer traces) or IAR/RW address (for data trace) matches that of the entered value will be printed. When a range is entered, the trace events that will be printed must have the appropriate address within the specified range.

Example (data trace previously declared):

```
**EDIT**
EDIT (L,D,A,R,N) = <A> <ETX>
ADDR (IAR,RW) = <IAR> <ETX>
ADDR = <12345> <ETX>
ETC.
```

Example (instruction trace previously declared):

```
**EDIT**
EDIT (L,D,A,R,N) = <A> <ETX>
ADDR = <R12345:6789A>
ETC.
```

where: ADDR value can be from 1 to 10 hexadecimal characters, right-justified.

(d) DATA = <Value> <ETX>

The DATA prompter specifies the data value that will be used to search the trace buffer and allow printout. Data can be specified from 1 to 8 hexadecimal characters, right justified. The data value specified will be compared against that of the general register contents (instruction or transfer traces) or the read/write data (data trace). Upon a match, the trace event will be printed.

Example:

EDIT

EDIT (L,D,A,R,N) = <D> <ETX>

DATA = <12345678> <ETX>

ETC.

where: Data value can be 1 to 8 hexadecimal characters.

(e) MASK = <Value; <ETX;;>

This step occurs only when a DATA EDIT is specified in step (a). The MASK feature allows the user to classify various bit positions as DON'T CARE. The MASK consists of 32-bit positions, specified by 1 to 8 hexadecimal characters (same scheme as monitored system), where placing a 1 in a bit position will mark it as a "DON'T CARE." If the user does not require the MASK feature, he may simply enter an ETX without specific data in step (d).

Example 1:

EDIT

EDIT (L,D,A,R,N) = <D> <ETX>

DATA = <12345678> <ETX>

MASK = <0000FFFF> <ETX>

Example 2:

EDIT

EDIT (L,D,A,R,N) = <D> <ETX>

DATA = <12345678> <ETX>

MASK = <ETX>

(f) GR = <Value> <ETX>

This step occurs only if a register edit is specified in step (a). This prompter allows the user to enter a general register number, from 0 to 7, for which trace events will be printed. Both full- and half-register change trace events will be printed.

Example:

EDIT

EDIT (L,D,A,R,N) = <R> <ETX>

GR = <1> <ETX>

HITS Command

5.10 The monitor command HITS, when entered, requests the number of hits (trace events) received after the start event occurs. However, if HITS is requested after the stop event occurs, the number of hits printed will be zero.

Example:

<STX>

I* <HITS> <ETX>

123

where: Value indicates number of hits in hexadecimal.

STOP_Command

5.11 The monitor command STOP, when entered during program execution, simulates a stop event, causing the trace buffer dump to be initiated.

Example (instruction trace):

<STX>

I* <STOP> <ETX>

LINE	EVENTS	FR-ADR	TO-ADR	GR	GR-DATA
0001	0001F	00045	00046	5	12345678
0002		00046	10000	7R	5678
0003		10000	10001	3L	1234

ETC.

Example (data trace):

<STX>

I* <STOP> <ETX>

LINE	EVENTS	IAR	R/W-ADR	DATA	OP TYP
0001	001F	0015F	001FF	01234567	100 01
0002		0015F	00200	89ABCEFF	100 01
0003		00160	00200	89ABCEFF	000 01

GO_Command

5.12 The monitor command GO restarts the trace buffer dump if it was previously interrupted, such as when the user enters a STX control character during a trace buffer dump (refer to paragraph 4.34).

Example:

LINE	EVENTS	FR-ADR	TO-ADR	GR	GR-DATA
0001	0800	00020	00042		
0002		00042	00043		
0003		00043	00044	1	2A52A5AF

<STX> (Trace Dump Interrupted)

I* <GO> <ETX> (Re-enable Trace Dump)

LINE	EVENTS	FR-ADR	TO-ADR	GR	GR-DATA
0004		00044	00047	2L	2A52
0005		00047	00048	2R	A5AF

ETC.

where: < > specifies user's input.

RESTART Command

5.13 The monitor command RESTART will reenable a trace operation using the same data previously entered via the TRACE command. Any EDIT option previously specified will still apply. However, auto-restart will not be reenabled by a RESTART command if it was in effect the last time a trace was performed. The only way to enable auto-restart is to go through a READY prompter, such as after performing a MODIFY X command.

Example:

<STX>

I* <TRACE> <ETX>

TRACE

.

.

.

READY (Y,N,E,X,A) = <Y> <ETX>

.

.

.

<STX>

I* <RESTART> <ETX>

where: < > specifies user's input.

DUMP_Command

5.14 The monitor command DUMP, allows the user to dump either a single trace event or a range of trace events. The VALUE is expressed in hexadecimal (ranging from 1 to 800) and indicates the line number of the printout.

DUMP <VALUE> <ETX> or <RANGE> <EXT> <COMMAND>

Example:

<STX>

I* <DUMP 100:200> <ETX>

LINE	EVENTS	FR-ADR	TO-ADR	GR	GR-DATA
0100	0200	10041	10042	4	44444444
0101		10042	10043	5L	5555
0102		10044	10045	6R	6666
.		.	.	.	.
.		.	.	.	.
.		.	.	.	.
0200		10242	10243	7	77777777

REG0	REG1	REG2	REG3	REG4	REG5	REG6	REG7
XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	44444444	5555XXXX	66666666	77777777

NOTES:
1. The register summary will reflect the most recent general register information, in the trace buffer, within the specified dump parameter.
2. X's in the register summary indicate that the general register contents, either full or half, did not change within the specified dump parameter.
3. There must be a space between DUMP and the first character of the value specified.
4. ~~< > specifies user's input.~~

MODIFY X Command

5.15 The monitor command MODIFY X enables the user to respecify trace setup data without having to reenter the monitor command TRACE and provide information for all prompter questions. The value X represents the TRACE prompter line number.

Example:

<STX>

I* <TRACE> <ETX>

TRACE

1 COPY (0,1,B) = <ETX>

2 MODE (P,R) = <P> <ETX>

3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = <PS><ETX>

READ-WRITE(R,W,B) = <ETX>

4 START(ADDR,EXT,IMMED) = <IMMED> <ETX>

5 STOP(ADDR,EXT,OVFL) = <OVFL> <ETX>

6 IAR RANGE = <ETX>

EVENTS = <FF> <ETX>

READY(Y,N,E,X,A) = <N> <ETX>

MONITOR

<STX>

I* <MODIFY 4> <ETX>

4 START(ADDR,EXT,IMMED) = <ADDR> <ETX>

START ADDR = <R0:1FF> <ETX>

EVENT CAPTURE (A,Q) = <A> <ETX>

DATA = <ETX>

EVENTS = <FF> <ETX>

READY(Y,N,E,X,A) = <Y>

NOTES: 1. The MODIFY X Command changed the start event from IMMED (System Monitor program control) to an address range of 0 to 1FF.

2. <> specifies user's input.

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BTEST N Command

5.16 The monitor command BTEST N initiates an internal test of portions of the system monitor hardware. The test consists of loading the trace buffer with various static and dynamic test patterns through the trace data multiplexer. Testing verifies the major data paths used in capturing trace data and associated control paths.

5.17 The test is divided into five separate phases with one phase associated with each buffer array card (FB-15671). The value of N can range from 0 to 5 and indicates the following:

N Phase	Microprocessor Address Range	Buffer Array File Location
1	2000 - 2FFF	B24
2	4000 - 4FFF	B26
3	6000 - 6FFF	B28
4	8000 - 8FFF	B30
5	A000 - AFFF	B32

If zero (0) is entered for the value N, all five phases will be executed.

Example:

```
<STX>
I* BTEST 0 <ETX>
BTEST: 01
ATP
BTEST: 02
ATP
BTEST: 03
ATP
BTEST: 04
```



ATP

BTEST: 05

ATP

MONITOR

5.18 If an error is detected during the test, the following data is printed for each faulty trace location:

(a) Address of faulty trace buffer location.

(b) Data pattern sent to trace buffer location (CP-correct pattern).

(c) Data pattern read from trace buffer location (FP-failing pattern).

The user can interrupt the printout of the faulty trace buffer locations by entering an STX control character (refer to paragraph 4.34).

Example:

<STX>

I* BTEST 0 <ETX>

BTEST: 01

ATP

BTEST: 02

ADDR	CP	FP
4000	55	54
4001	55	54
4002	55	54

<STX>

BTEST: 03

ATP

BTEST: 04

ETC.

LOAD Command

5.19 The monitor command LOAD indicates to the program to perform a memory reload from the magnetic tape cartridge. This command allows a user, at a remote location, to perform a program reload via the keyboard terminal if he suspects a fault with the operational program. This command assumes that certain portions of the operational program are intact when the command is issued.

Example:

<STX>
I* <LOAD> <SUB> <ETX>
(PROGRAM LOAD COMPLETE)
LOAD OK
BAUD RATE (10, 30, 120) = <Selection> <ETX>
BTEST: 01
ATP
.
.
.
BTEST: 05
ATP

where: SUB represents a CTL-Z entry on the keyboard terminal.
<-> denotes user's input.

Trace Examples

5.20 Figure 6 shows the trace memory word format for instruction, transfer and data traces.

5.21 Instruction Traces (Figures 7 through 12). Figure 7 illustrates a progressive instruction trace setup and dump of the address of the last instruction executed, with general register changes, beginning at the start address of 1400. The stop event is trace buffer overflow and only 20 events are to be printed. Lines 0003 and 0004 of the trace dump indicate that a multiple CP operation occurred. The first CP operation (line 0003) was a general register change, and the second (line 0004) was the instruction decode. The general register summary at the end of the dump is the contents of the registers after the selected first 20 events.

5.22 Figure 8 is an INS trace depicting the SMI instructions executed and the resulting trace dump. Note the TBZ loop starting at line 0017.

5.23 Figure 9 depicts the edit mode loop inhibit feature using the trace setup of the previous example. The printout of the loop address was inhibited at line 001B as indicated by the *.

5.24 Figure 10 illustrates a macroinstruction trace setup and resulting trace dump for an execute instruction (XEC), which is a transfer instruction (TPR) to another section of SMI code.

5.25 Figure 11 is an example of a modification of the previous trace example (Figure 10). The modification is to specify a range for the start address and to trace only those addresses within the specified range.

5.26 Figure 12 illustrates another modification of the INS trace example in Figure 10. This modification specifies a range for the start address and traces all addresses after the start address range is detected.

5.27 Transfer (XFR) Trace. Figure 13 illustrates a regressive XFR trace with the start trace program address of 2988 and the stop address of 294D. The event capture response of A specifies to capture all events after the match on the start address. Ten (10) events were specified but only E events were captured to meet the start/stop conditions.

5.28 Instruction Store (IS) Data Traces (Figures 14 through 20). Figure 14 depicts a progressive IS trace for read instructions (RIS) of IS memory that are executed within the range of program addresses (IAR) 2795 to 2A27.

5.29 Figure 15 depicts an IS address of 2A91 for the trace start event and address 2A70 for the stop event. The trace begins upon detection of the specified start address, and all events thereafter that occur within the IAR range of 27A8 to 27B6 will be captured until the stop address is detected.

5.30 Figure 16 is an example of a modification of the previous trace (Figure 15). The modification was to the start address EVENT CAPTURE to qualify (Q) the trace capture to detect only the starting address specified.

5.31 Figure 17 is another modification of the trace example of Figure 15 in which the START event detection is specified by a start address 2A91 and a data pattern of 00202A6E, and the EVENT CAPTURE of A specifies to trace all events when the specified start conditions are detected. This type of trace can be used when the IS address and data content are known, and the IAR is desired.

5.32 Figure 18 specifies a start event IS address range in which the left half of the data contents specified and the right half are irrelevant. This type of trace can be used to trace a software register in which a specific data pattern, such as a Network Inlet Terminal (NIT) or hardware circuit identity is known and the IAR is desired.

5.33 Figure 19 specifies an outside range of IS memory in which only those IS events that occur outside the specified range are captured.

5.34 Figure 20 specifies an IAR address range, and only those IS events that occur outside of the specified IAR range are to be captured. This type of trace can be used when any IS operations are performed outside of a specified program module (IAR outside range).

5.35 Process Store (PS) Data Trace. Figure 21 depicts a PS data trace with a specified IAR address range. This type of trace should be used when the program module address range is known and the PS addresses and data are desired.

5.36 Memory Data Trace. Figure 22 is a typical trace of Memory (MEM) operations performed during normal program execution.

5.37 Peripheral Controller (PC) Data Trace. Figure 23 depicts a PC data trace with an IAR inside range specified. This type of trace should be used when a known program module (IAR inside range) is to be traced for any PC operations executed.

5.38 Command Bus Trace. Figure 24 depicts all activity on the command bus (CMD) that is executed within the program IAR address range. To the right of the trace dump is the bus operation and associated SMI. Note the multiple bus operations performed during the execution of one instruction.

5.39 Figure 25 depicts a command bus trace with request to dump more data stored in the trace buffer from the previous trace.

5.40 Direct Memory Access (DMA) Data Trace. Figure 26 depicts a DMA trace that was executed while memory was being loaded through the DMA channel from a PDP/GPIO.

5.41 Edit Options. Figures 27 through 35 illustrate various uses of the edit feature. Figures 27 through 31 are referenced to the DMA trace in Figure 26.

5.42 HITS/STOP Commands. Figure 36 illustrate the use of the HITS and STOP commands.

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6. X-RAY MICRODIAGNOSTICS

General Operation and Characteristics

6.01 The primary function of the system monitor X-ray microdiagnostics is to test the common control system during start-up. Microdiagnostic programs verify internal processor functions in a sequential manner, from very basic to complex functions. Analysis of X-ray program execution is more accomplished by a system monitor trace that is manually set up before X-ray execution.

6.02 Operation. Microdiagnostic programs are loaded from the system monitor magnetic tape cartridge facility into a high-speed ROMSIM. This ROMSIM is physically attached to one of the three CP's; the other two CP's are disabled. Upon suitable commands, the ROMSIM is enabled, the CP performs actions directed by the microdiagnostic, and the system monitor captures data in its trace memory. The captured data may then be analyzed to determine if the micro-instructions were executed correctly.

6.03 Before loading a microdiagnostic, the type of information to be captured is established by setting up a system monitor trace operation via the TRACE command. Trace parameters such as the bus copy to be monitored, type of trace to be performed, start/stop address range or data, and the various edit options are entered at this time. After entering the X-ray control mode from the TRACE mode by inputting an X-RAY command, the user may enter various additional sequence control and data parameters that may be required. These entries are diagnostic-dependent and are part of the operator instructions for each micro-diagnostic program.

6.04 After a microdiagnostic is loaded and execution is started, the user can use various monitor commands to stop data capture, and then to change the type of information being captured, edit the data already captured, or restart the trace data capture. While the operator is making trace parameter changes, the microdiagnostic continues to run and can only be stopped if the X-ray control mode is reentered. Thus, it is not necessary to reload a tape cartridge each time the trace parameters are changed; it is necessary to reload only if a new microdiagnostic is to be executed.

6.05 Entry to the X-ray control mode can also be made by entering an X-RAY on the keyboard as a discrete command. However, this can only be done if the X-ray control mode has been entered previously via the TRACE command mode. Upon any entry into the X-ray command mode, the attached CP is ~~found~~ forced into the STOP mode until the X-ray command mode is exited.

6.06 The first time the X-ray control mode is entered, an X-ray self-test is executed upon any ROMSIM cards that are installed.

6.07 X-ray Data Capture. During the execution of X-ray microdiagnostics, the system monitor can capture data from the following four sources: the CP general registers, the Next Execute Program Counter (NEPC), the micro-instruction address, and the system command and system response buses. Data cannot be captured in the trace memory from all four sources simultaneously; all data is sampled, but which data is saved depends on the trace and X-ray setup information specified by the user. Data is captured as follows:

(a) General register data capture. The system monitor captures changes to the CP general registers by monitoring the control and data inputs to the A file. Any changes to file A, registers 0 through 8, are captured. Changes to register 0 or register 8 are both saved as changes to register 0. Changes to file A, registers 9 through F, or to any file B registers

are ignored by the system monitor. Sixteen-bit changes to the upper or lower half-register or 32-bit full-register changes can be captured. Thus, when a general register change is detected, the register number (0 through 7), the portion modified (upper, lower, full), and the changed data (16 or 32 bits) are captured.

(b) NEPC data capture. The system monitor samples the contents of the NEPC whenever a decode is performed by the CP. Changes to the NEPC between decodes are not ~~deleted~~ detected by the system monitor; however, the CP control signal used to load the NEPC serves as an indicator flag to the system monitor that a transfer instruction is in process. Because the NEPC is traced by the system monitor only at decode time, and because decodes are not normally performed during microdiagnostics, changes to the NEPC may be of limited value during X-ray microdiagnostic execution.

(c) Microinstruction address data capture. During microdiagnostic execution, the microlocation from which the next microinstruction is to be accessed is generated by the CP-under-test, latched at the X-ray buffer board, driven to the X-ray control board, and converted to an address for the X-ray ROMSIM cards. Registers on the X-ray control card sample the microinstruction address and delay it until data from the microinstruction execution is assembled by the system monitor trace facilities. Data selection logic provided within the system monitor allows the user to select either the macroinstruction address or microinstruction address to be traced. The microinstruction address can be traced at every microinstruction cycle or traced only when a general register change occurs.

(d) System command bus and system response bus data capture. The bus command field of the CP microinstruction word is used by a scheduling algorithm implemented in the system monitor hardware to sample data from the system

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command bus and system response bus. The basic function of the scheduling algorithm is to capture a logical address from the system command bus along with internal CP page bits and to associate this logical address with appropriate data from either the system command bus (for write operations) or from the system response bus (for read operations). When the address and data information is assembled, the bus command code is compared to trace setup information to decide if the address and data should be saved in the trace memory or ignored. Table 1 shows which bus command codes allow address and data to be saved in the trace memory based upon trace setup information.

NOTE: Only the lower 16 bits of the system command bus are sampled for address information, whereas 32 bits are sampled for data either from the command bus or response bus. Also, the system monitor can selectively monitor either bus 0, bus 1, or both buses. Each bus can be used to pass different information to the system monitor during microdiagnostic execution, with the user deciding which information is to be monitored by selecting the appropriate bus copy. The address and data matchers can similarly be used to selectively pick out a desired subset of bus information.

6.08 X-ray trace control flags. The CP is equipped with a firmware control flag that can be used to start or stop a system monitor trace. This flag, FRCOV, can be set or reset directly by the CP microinstruction through the V-flop control field. Two additional inputs, EXT1 and EXT2, are available at the SMI interface card which can be strapped to CP backplane pins to facilitate control trace starting and stopping. Normally, these external inputs are not used.

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6.09 X-ray microdiagnostic structure. For analysis and usage of microdiagnostics, the following features are provided: standardized usage of the general registers; dedicated microlocations for starting or stopping, both normal and abnormal; and fixed locations for user-alterable sequence control and parameters.

X-RAY Command Description

6.10 The X-RAY command is used for controlling the X-ray subsystem of the System Monitor. Entry to the X-ray control can be made via the TRACE command by responding with an X to the READY prompter question, or by entering, via the keyboard terminal, the monitor command X-RAY.

Example 1: Assumes that the X-RAY command is entered for the first time.

4 START(ADDR,EXT,IMMED) = <IMMED> <ETX>

5 STOP(ADDR,EXT,OVFL) = <OVFL> <ETX>

EVENTS = <5> <ETX>

READY(Y,N,E,X,A) = <X> <ETX>

X-RAY

X-RAY MAX SIZE = 1K

XTEST: 01

ATP

X-RAY (S,L,E,EM,I,T,P,C) = <Selection> <ETX>

Example 2: Assumes that the X-RAY command mode was entered previously.

<STX>

I* <XRAY> <ETX>

X-RAY

X-RAY(S,L,E,EM,I,T,P,C) = <Selection> <ETX>

~~where: < > specifies user's input.~~

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6.11 If the TRACE command setup is being performed before execution of an X-ray microdiagnostic, the following restrictions and suggestions regarding the selection and use of trace parameters should be noted:

(a) Type of trace. Unless otherwise directed by the microdiagnostic documentation, the only trace mode to be used in the Instruction (INS) trace mode, with microinstruction addresses selected instead of macro-instruction addresses.

(b) Start/Stop events. The CP-under-test microaddress may be selected for use instead of the macroaddress program counter.

(c) Auto-restart. If a microdiagnostic is executed in the auto-restart mode, the attached CP is stopped and execution forced to begin at microlocation 0 before each new trace is initiated. However, the microdiagnostics are not restarted at microlocation 0 when the RESTART command is used.

6.12 Following an X-RAY entry on the keyboard, a prompter question listing further X-ray command choices occurs. Example:

X-RAY (S,L,E,EM,I,T,P,C) = <Selection> <ETX>

where:

S = Size	Used for specifying how much X-RAY ROMSIM is available.
L = Load	Used for loading microdiagnostics into X-RAY ROMSIM.
E = Execute	Used to initiate normal microdiagnostic execution.
EM = Execute Modified	Used to initiate special microdiagnostic execution.
I = Inspect	Used to selectively printout and/or change portions of the ROMSIM.

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T = Test	Used to perform an X-ray self-test.
P = Parameter Update	Used to modify the microdiagnostic parameter table.
C = Control Update	Used to modify the microdiagnostic sequence control table.

6.13 After selection of one or more of the above X-RAY commands, the X-ray control program generates additional prompter questions. Each of these commands is discussed below, along with the ensuing prompter questions.

6.14 Size (S). The following prompter question occurs after an S selection on the X-RAY command:

X-RSIZE (1,2,3,4) = <Selection> <ETX>

This question requires the user to respond with the size of the ROMSIM array to be used for microdiagnostics. The possible responses are: 1 (1K), 2 (2K), 3 (3K), or 4 (4K). If the user responds with a size greater than the available ROMSIM size, a message is outputted specifying the maximum ROMSIM size. The size prompter question is then reissued.

Example:

X-RAY (S,L,E,EM,I,T,P,C) = <S> <ETX>

X-RSIZE (1,2,3,4) = <2> <ETX>

X-RAY MAX SIZE = 1K

X-RSIZE (1,2,3,4) = <1> <ETX>

X-RAY (S,L,E,EM,I,T,P,C) =

6.15 Load (L). In response to the selection of a microdiagnostic loading (L) command, the control program verifies that a microdiagnostic cartridge is installed in the magnetic data cartridge reader. Possible output messages are as follows:

(a) If the cartridge has not been loaded, the following message is outputted and repeated until the user installs a cartridge:

CARTRIDGE IS OUT

(b) If a cartridge has been installed, the following message is outputted:

CARTRIDGE IN OK -- REWINDING

(c) After the message in 6.15 (b) above is outputted, the header on the tape is printed out for user inspection, and the data following the header is loaded into ROMSIM. After the data is loaded, the tape rewinds and a verify of ROMSIM data compared to tape data is performed. The following message is outputted:

VERIFY STARTED

(d) If errors are detected during reading of the tape, the following message is ~~be~~ printed:

***CRC ERROR DURING READ OF RECORD #X

(e) If an error is detected during verify, the following message ~~will be~~ is printed:

***MIS-MATCH ERROR DURING VERIFY -- RECORD #X

BYTE # XX

ROMSIM DATA = YY

TAPE DATA = ZZ

(f) After a successful tape load and verify, the following message is printed and the X-RAY command is reprompted:

VERIFY COMPLETE

Example:

```
X-RAY (S,L,E,EM,I,T,P,C) = <L> <ETX>
**CARTRIDGE IN OK -- REWINDING**
SEQUENCE TEST 9-10-77 VER 2.1
**VERIFY STARTED**
**VERIFY COMPLETE**
X-RAY (S,L,E,EM,I,T,P,C) = <E> <ETX>
ETC.
```

6.16 Execute (e) and Execute Modified (EM). There are two types of X-RAY executions:

(a) A normal X-ray microdiagnostic execution is initiated by entering an E when the basic X-RAY command is presented. During normal microdiagnostic execution, the microinstruction address is traced instead of the macroinstruction address and is only captured when a general register change occurs. Normal microdiagnostic execution requires that the instruction trace mode be selected during trace setup. All prompter question references to instruction address during the trace setup should be interpreted as microinstruction address rather than macroinstruction address. When the E is typed, the attached CP is allowed to RUN, starting at microlocation 0. Once execution has begun, control is passed to the operational control program. A trace is initiated by using the previously specified trace parameters, and data is captured in the trace buffer. The attached CP executes the microdiagnostic continuously until the X-ray control mode is entered again. If the auto-restart mode is selected during trace setup, as each new trace is started the attached CP is forced to restart microdiagnostic execution at microlocation 0.

(b) A modified X-RAY execution is initiated by entering an EM when the basic X-RAY command is presented. In this case, the user may select either macroinstruction or microinstruction addresses to be traced. If microinstruction addresses are selected, the user may then choose to capture the addresses every microcycle or for reference only when a general register change occurs. These options are selected via the two following prompter questions that are generated after an EM command input:

(1) ADDRESS TYPE(MICRO,MACRO) = <Selection> <ETX>

where:

A MICRO response selects the microinstruction addresses as a traceable parameter. All references to instruction addresses in the trace setup description should be interpreted as microinstruction addresses. The microprocessor is normally selected for microdiagnostic execution.

A MACRO response selects the macroinstruction addresses as a traceable parameter. Tracing of macroinstruction addresses may be required for specific microdiagnostics of the instruction decode features of the attached CP. The MACRO selection should not be made unless directed by the microdiagnostic setup documentation.

(2) MICRO ADDR EVENT (FORCE,REF) = <Selection> <ETX>

This prompter question only occurs if MICRO is chosen above. A FORCE response results in the microinstruction address being traced every microcycle and is used when microdiagnostics are used to check the basic sequencing logic of the CP. A REF response results in the microinstruction address being captured only when a general register change is detected. This mode is the normal setup for tracing microaddresses during microdiagnostic execution.

6.17 Inspect (I). The X-ray control program can read and modify selected portions of a microdiagnostic that was loaded into the ROMSIM. This feature is activated only by the I response to the basic X-ray command. The following prompter question then occurs:

X-INSPECT ADDR = <Value> <ETX>

6.18 There are two valid responses for the X-INSPECT ADDR prompter:

(a) If a single hexadecimal address parameter (one to three characters, right justified) is entered, the corresponding ROMSIM location is printed, followed by a dash (-). To modify the contents of this ROMSIM location, a 12-character hexadecimal parameter should then be entered, followed by an ETX. This causes the inspect program to advance to the next ROMSIM location, print out the contents (followed by a dash), and to wait for a new entry. If no modification ~~is~~ is desired, a slash (/) should be entered, followed by an ETX. This preserves the current location and advances to the next microlocation for printout. To terminate the inspect/change operation, an ETX with no data should be entered after the dash on the microlocation printout. After the ETX is entered, the basic X-RAY command prompt will be reissued.

Example:

X-RAY (S,L,E,EM,I,T,P,C) = <I> <ETX>

X-INSPECT ADDR = <0> <ETX>

0000 23456789ABCD - <123456789ABC> <ETX>

0001 123456789ABC - <23456789ABCD> <ETX>

0002 25F8212E39C0 - <456789ABCDEF> <ETX>

0003 13D80C942141 - </> <ETX>

0004 57EEF7518D92 - <ETX>

X-RAY (S,L,E,EM,I,T,P,C) = <I>

ETC.

00054

(b) If two hexadecimal address parameters (each one to three characters, right justified) separated by a colon are entered for the X-INSPECT ADDR, the corresponding ROMSIM locations are printed. The basic X-RAY command prompter is reissued after the selected microlocation printout is completed.

Example:

```
X-RAY (S,L,E,EM,I,T,P,C) = <I> <ETX>
X-INSPECT ADDR = <0:4> <ETX>
0000 123456789ABC
0001 23456789ABCD
0002 456789ABCDEF
0003 13D80C942141
0004 57EEF7518D92
X-RAY (S,L,E,EM,I,T,P,C) =
```

6.19 If a non-hexadecimal character, or if more than 12 characters are entered while changing a microlocation, three question marks are printed and the contents of the microlocation retyped for correction.

Example:

```
X-RAY (S,L,E,EM,I,T,P,C) = <I> <ETX>
X-INSPECT ADDR = <0> <ETX>
0000 123456789ABC - <RSUT> <ETX>  ???
0000 123456789ABC - <23456789ABCD> <ETX>
0001 456789ABCDEF - <56789ABCDEF12> <ETX>  ???
0001 456789ABCDEF - <56789ABCDEF1> <ETX>
0002 789ABCDEF123 - <ETX>
X-RAY (S,L,E,EM,I,T,P,C) =
```

6.20 Test (T). An X-RAY self-test consists of loading the ROMSIM with various patterns and reading them back through the 8080 interface. All ROMSIM's installed in the system, up to a maximum of 4K, are tested. The X-ray test is divided into four phases, each associated with a 1K page of ROMSIM. The portions of ROMSIM tested according to phase and microprocessor address range are shown in Table 2. A self-test is automatically performed the first time the X-ray control mode is accessed after the operational control program is loaded.

6.21 After entry of a T subcommand, the following prompter question occurs:

X-TEST (0,1,2,3,4) = <Selection> <ETX>

If a 0 is entered, ~~for the selection~~, all available ROMSIM will be tested. At the beginning of the self-test, a message will be printed informing the operator of the maximum size of the ROMSIM installed. Upon completion of the self-test, the basic X-RAY command will be reissued.

If a specific page is selected, only that page will be tested.

Example:

X-RAY (S,L,E,EM,I,T,P,C) = <T> <ETX>

X-TEST (0,1,2,3,4) = <0> <ETX>

X-RAY MAX SIZE = 1K

XTEST: 0

ATP

X-RAY (S,L,E,EM,I,T,P,C) =

6.22 If an error is detected during the test, the following data is printed for each faulty ROMSIM location:

(a) Address of faulty ROMSIM location.

(b) Data pattern sent to ROMSIM location (CP-correct pattern).

(c) Data pattern read from ROMSIM location (~~FP~~ CP-failing pattern).

6.23 The user can interrupt the printout of the faulty ROMSIM locations by entering a STX.

Example:

X-RAY (S,L,E,EM,I,T,P,C) = <T> <ETX>

X-TEST (0,1,2,3,4) = <0> <ETX>

X-RAY MAX SIZE = 1K

XTEST: 01

ADDR	CP	FP
1000	AA	2A
1001	AA	2A
1002	AA	2A
1000	FF	7F
1001	FF	7F
1002	FF	7F

STX

X-RAY (S,L,E,EM,I,T,P,C) =

00057

6.24 The following example combines the X-ray self-test and magnetic tape cartridge load procedures:

```
I* XRAY
     **X-RAY**
     X-RAY (S,L,E,EM,I,T,P,C) = T
     X-TEST (0,1,2,3,4) = 0
     X-RAY MAX SIZE = 1K
     XTEST: 01
     ATP
     X-RAY (S,L,E,EM,I,T,P,C) = L
     **CARTRIDGE IN OK -- REWINDING**
     MIUTST.B02 1-25-78
     **VERIFY STARTED**
     **VERIFY COMPLETE**
```

6.25 Parameter Update (P). The number of entries in the parameter control table and the meaning of the parameters are entirely microdiagnostic-dependent. The X-ray control program, however, provides a means of altering the data if required. An area of ROMSIM, starting at location 300, is reserved for microdiagnostic data that the user may have to alter.

6.26 The following prompter is generated in response to a P entry for the basic X-RAY command:

```
X-PARAM ADDR = <Value> <ETX>
```

The user is required to enter the hexadecimal number of the parameter to be modified. The entered number is compared to the contents of a microlocation that specifies the number of parameter table entries. If the entered number is valid, the four-character parameter is printed, followed by a dash (-). The program then waits for a new user entry of up to four hexadecimal characters followed by an ETX.

Example: Examine and Change Parameter

X-RAY (S,L,E,EM,I,T,P,C) = <P> <ETX>

X-PARAM ADDR = <1> <ETX>

0001 0000 - <234> <ETX>

0002 0000 - </> <ETX>

0003 0000 - <ETX>

X-RAY (S,L,E,EM,I,T,P,C) =

where: The number of parameters specified by the microdiagnostic is 4.

6.27 If the entered parameter number is greater than allowed by the microdiagnostic, a message will be outputted to the user and the X-PARAM ADDR prompt will be reissued.

6.28 A range of parameters can be displayed by entering two address parameters separated by a colon.

Example: Examine Range of Parameters

X-RAY (S,L,E,EM,I,T,P,C) = <P> <ETX>

X-PARAM ADDR = <0:3> <ETX>

0000 0000

0001 0000

0002 0000

0003 0000

X-RAY (S,L,E,EM,I,T,P,C) = <P> <ETX>

X-PARAM ADDR = <4:5> <ETX>

****ADDR OUTSIDE OF TABLE

X-PARAM ADDR = <0> <ETX>

0000 0000 - <ETX>

X-RAY (S,L,E,EM,I,T,P,C) =

where: The number of parameters specified by the microdiagnostic is 4.

6.29 Control Update (C). Two fixed microlocations have been defined in the microdiagnostic structure for X-ray sequence control of execution of up to 16 subtests (called phases) within a microdiagnostic. The actual number of subtests and control of these subtests are microdiagnostic-dependent. The user must refer to the appropriate microdiagnostic documentation for allowed sequence control information.

6.30 The following prompter is generated in response to a C entry for the basic X-RAY command:

X-SEQNCE ADDR = <Value> <ETX>

Valid responses are 0, 1, or 0:1, depending on the type of sequence control desired:

(a) A 0 entry causes the phase selection parameter to be printed, followed by a dash (-). The program then waits for a new user entry of up to four hexadecimal digits corresponding to the desired phase selection. Phase selection is determined by bit positions 0 through 15 (left to right) in sequence control word 0 with a 1 in a bit position, allowing the corresponding phase to RUN and a 0 causing the phase to be skipped. Thus, an entry of 8000 would RUN phase 0 and allow the remaining phases (1 through 15) to be skipped.

(b) A 1 entry causes the loop control parameter to be printed, followed by a dash (-). The program then waits for a new entry of up to four hexadecimal digits corresponding to the desired loop selection. In the loop control word, a 0 in a bit position will inhibit looping on the corresponding phase; a 1 in a bit position will cause the microdiagnostic to loop on the phase corresponding to the bit position when the phase is executed. Thus an entry of 4000 will cause the microdiagnostic to loop on phase 1.

00060

(c) A 0:1 entry followed by an ETX causes both the phase selection and loop control parameters to be displayed.

(d) If an attempt is made to make an entry other than 0 or 1 for the X-SEQNCE ADDR, an error message will be printed and the X-SEQNCE ADDR reprompted.

Examples:

X-RAY (S,L,E,EM,I,T,P,C) = <C> <ETX>

X-SEQUENCE ADDR = <0:1> <ETX>

0000 FFFF - <1234> <ETX>

0001 FFFF - <2345> <ETX>

X-RAY (S,L,E,EM,I,T,P,C) = <C> <ETX>

X-SEQNCE ADDR = <2> <ETX>

***ADDR OUTSIDE OF TABLE

X-SEQNCE ADDR = <0:1> <ETX>

0000 1234

0001 2345

X-RAY (S,L,E,EM,I,T,P,C) =

Table 1. Bus Command Code Recognition.

BUS COMMAND CODE		DATA TRACE TYPE					
CREG 31-35	MEANING	IS	PS	MEM	DMA	PC	CMD
		SPIL07= 0	SPIL07= 1				
00	NOT USED	-	-	-	-	-	-
01	DMA-WRITE DATA	-	-	-	-	-	x
02	FETCH-UNCOND. XFR	-	-	x	-	-	x
03	WRITE DATA-FLIP	-	-	-	-	-	x
04	FETCH-EXECUTE	-	-	x	-	-	x
05	PIPELINE FETCH	-	-	-	-	-	x
06	FETCH IF ZERO	-	-	x	-	-	x
07	FETCH IF NZERO	-	-	x	-	-	x
08	READ - MEM. (MAPPED)	x	x	x	-	-	x
09	WRITE - MEM. (MAPPED)	x	x	x	-	-	x
0A	DMA DATA TO BDOR	-	-	-	-	-	-
0B	WRITE DATA	-	-	-	-	-	x
0C	READ - MEM. (MAPPED) SR	x	x	x	-	-	x
0D	WRITE - MEM. (MAPPED) SR	x	x	x	-	-	x
0E	READ NON. MEM	-	-	-	-	-	x
0F	WRITE NON. MEM	-	-	-	-	-	x
10	DMA-COMMAND	-	-	-	-	-	-
11	NOT USED	-	-	-	-	-	-
12	READ - MEM. (DIRECT) SR	-	-	x	-	-	x
13	WRITE - MEM. (MAPPED) SR	-	-	x	-	-	x
14	FETCH - MEM. (MAPPED) SR	-	-	x	-	-	x
15	REFRESH	-	-	x	-	-	x
16	DMA - READ MEM. (MAPPED)	-	-	-	x	-	x
17	DMA - WRITE MEM. (MAPPED)	-	-	-	x	-	x
18	PAU - ACCESS	-	-	-	-	x	x
19	SPECIAL PAU RTN	-	-	-	-	-	x
1A	DMA CMD TO BDOR	-	-	-	-	-	-
1B	WRITE DATA - EV. PAR.	-	-	-	-	-	x
1C	PAU - ACCESS SR	-	-	-	-	x	x
1D	WRITE - MEM. (MAPPED) W/O PROT.	x	x	x	-	-	x
1E	READ MAP	-	-	-	-	-	-
1F	LOAD MAP	-	-	-	-	-	-

NOTE: x = Allowed Bus Command Code for Data Trace Type
- = Bus Command Code Not Recognized

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TABLE 2. X-ray Self-Test.

TEST PHASE (PAGE)	MICROPROCESSOR ADDRESS RANGE	ROMSIM FILE LOCATION
1	0800 - 0FFF	A11
	1000 - 17FF	A13
	1800 - 1FFF	A15
2	0800 - 0FFF	A11
	1000 - 17FF	A13
	1800 - 1FFF	A15
3	0800 - 0FFF	A10
	1000 - 17FF	A12
	1800 - 1FFF	A14
4	0800 - 0FFF	A10
	1000 - 17FF	A12
	1800 - 1FFF	A14

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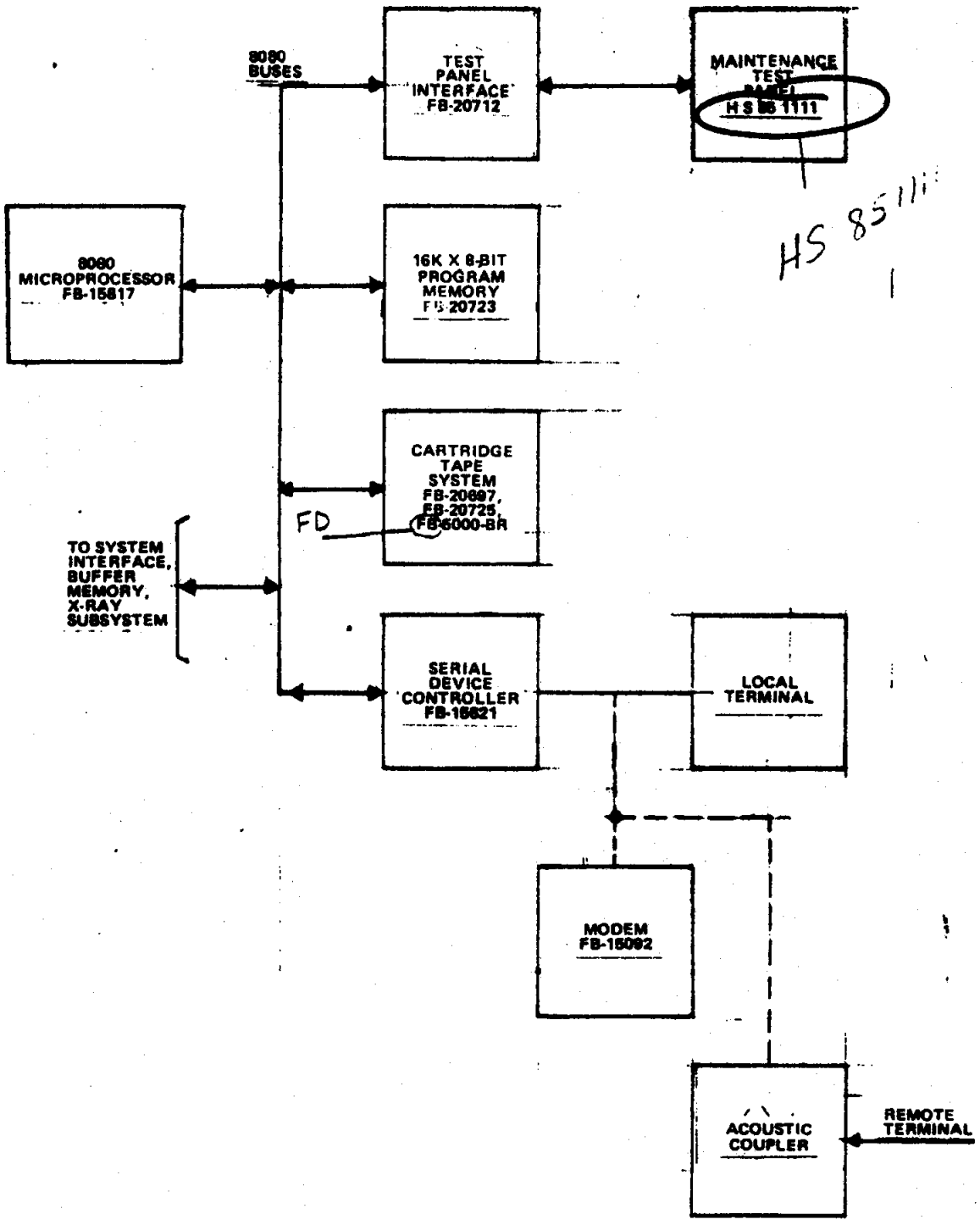


Figure 1 Monitor Control.

00064

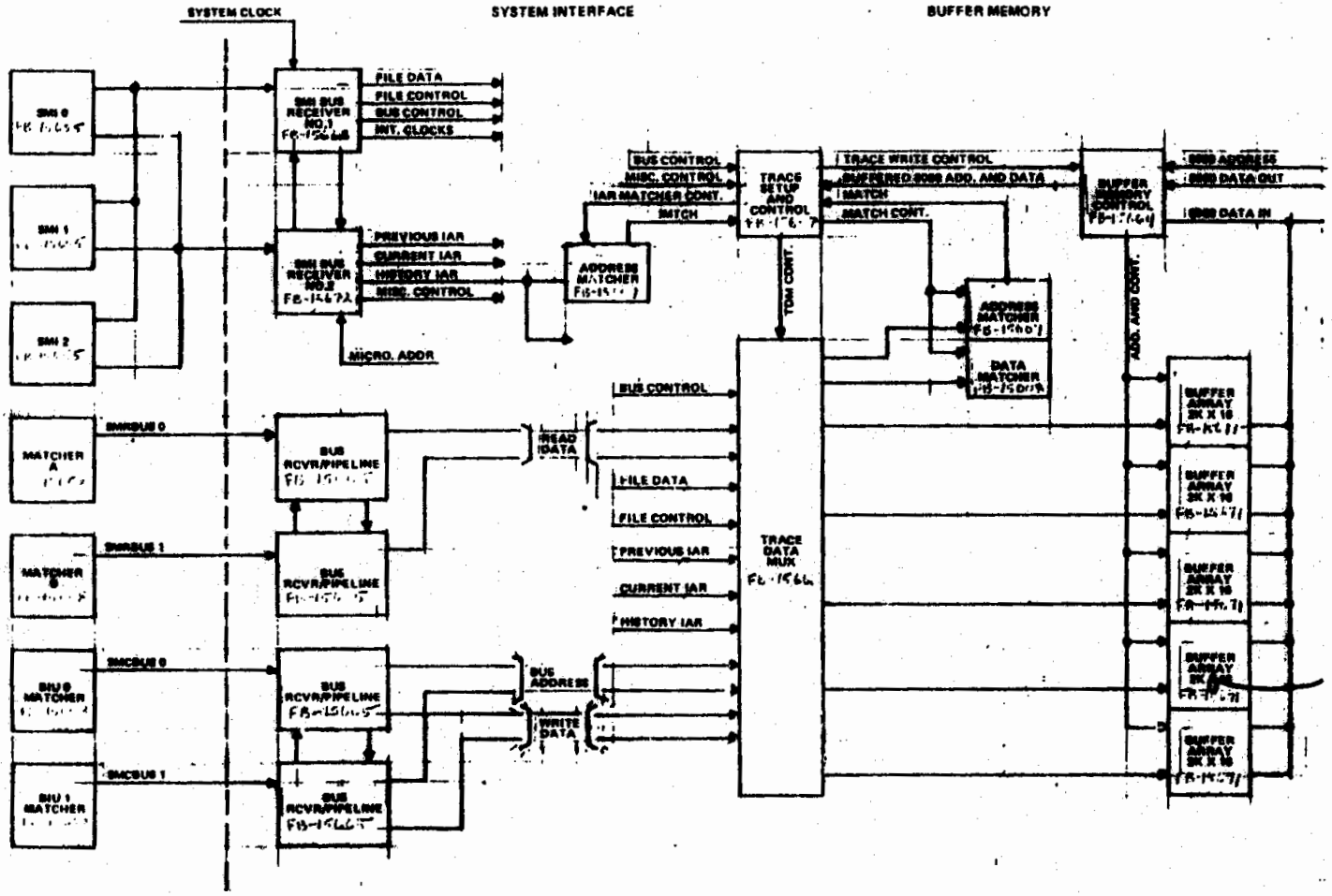


Figure 1. System Monitor - System Interface and Buffer Memory.

00065

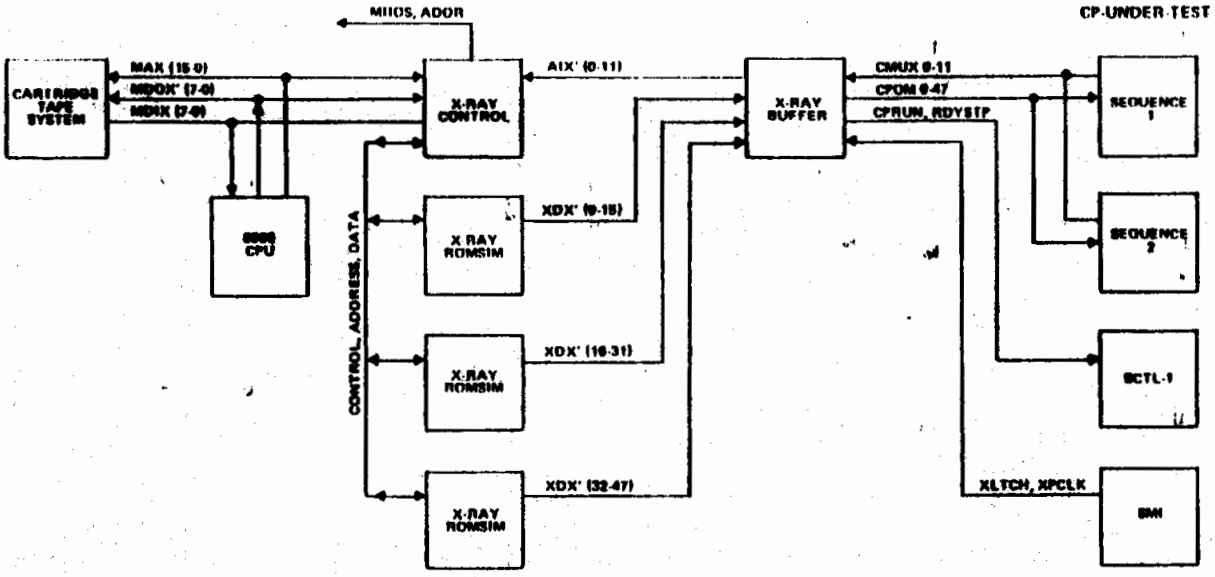


Figure 3. X-ray Block Diagram.

00066

SELECTED START EVENT \ POSSIBLE STOP EVENT	Exact Address B (no data)	Exact Address B (data with mask)	Address within A:B (no data)	Address within A:B (data with mask)	Address outside A:B (no data)	Address outside A:B (data with mask)	External Event 1	External Event 2	Firmware Flag (FRCOV)	Buffer Overflow
Exact Address A (no data)	√						√	√	√	√
Exact Address A (data with mask)		√					√	√	√	√
Address within A:B (no data)							√	√	√	√
Address within A:B (data with mask)							√	√	√	√
Address outside A:B (no data)							√	√	√	√
Address outside A:B (data with mask)							√	√	√	√
External Event 1	√	√	√	√	√	√		√	√	√
External Event 2	√	√	√	√	√	√	√		√	√
Firmware Flag (FRCOV)	√	√	√	√	√	√	√	√		√
Program IMMED	√	√	√	√	√	√	√	√	√	√

Note: √ = Allowed Event Combination

Figure 4. Start/Stop Event Selection.

00067

OP \ TYP	NON-MEMORY	PS MEMORY	IS MEMORY	UNMAPPED MEMORY
	00	01	10	11
000	READ	READ PS	READ IS	READ MEM
001	ACCESS PAU READ	DMA READ PS	DMA READ IS	-
010	RETURN PAU	-	FETCH IS	-
011	-	-	PIPELINE FETCH IS	-
100	WRITE	WRITE PS	WRITE IS	WRITE MEM
101	ACCESS PAU WRITE	DMA WRITE PS	DMA WRITE IS	-
110	WRITE DATA	-	-	-
111	-	-	-	REFRESH

FORMAT: OP TYP

XXX XX

Figure 5. Bus Operation Codes for System Monitor Data Traces.

Figure 6.

00069

```
** TRACE **
1 COPY(0,1,B)=0
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=INS
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=1400
EVENT CAPTURE (A,Q)=A
5 STOP(ADDR,EXT,OVFL)=OVFL
EVENTS=20
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  0800  016CF  01400  7R      16D1
0002        01400  01401  0L  0019
0003        01401  01402  7   00191403
0004        01401  01402
0005        01402  00980
0006        00980  00981
0007        00981  00982
0008        00982  00983
0009        00983  00984
000A        00984  00985
000B        00985  00986  0L  0019
000C        00985  00986
000D        00986  01403  5   000C0001
000E        01403  01404  4L  0BC4
000F        01404  01405
0010        01405  01406
0011        01406  01407
0012        01407  0140A
0013        0140A  0140B  6L  0602
0014        0140B  0140C
0015        0140C  0140D
0016        0140D  0140E  5   000C0001
0017        0140E  0140F  4   002017F6
0018        0140F  01410  4L  17F6
0019        01410  01411
001A        01411  01412  3   002017F6
001B        01412  01413  2L  001F
001C        01413  01414  1L  0000
001D        01414  01415
001E        01415  01416
001F        01416  01417
0020        014017  01418  6L  0700

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0019XXXX 0000XXXX 001FXXXX 002017F6 17F617F6 000C0001 0700XXXX 00191403
```

Figure 7. Trace Setup and Dump of Last Instruction Address Executed.

00070

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=INS
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=B936
EVENT CAPTURE (A,Q)=A
5 STOP(ADDR,EXT,OVFL)=OVFL
EVENTS=20
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA       SMI TRACED

0001  0800  09EC4  0B936  4   00000000       RPS  0L,4F
0002        0B936  0B937  5   00000000       RPS  0L,5F
0003        0B937  0B938  4R      0000       ISP  5F,4F
0004        0B937  0B938  4L  0000
0005        0B938  0B939  5   00000000       RPS  0L,5F
0006        0B939  0B93A  4R      0000       ISP  5F,4F
0007        0B939  0B93A  4L  0000
0008        0B93A  0B93B  2R      0000       CPY  SP,2F
0009        0B93A  0B93B  2L  8D14
000A        0B93B  0B93C  1L  0D14           CHA  2L,1L
000B        0B93C  0B93D                     CPH  1L,0L
000C        0B93D  0B93E                     TBZ  0L,0F
000D        0B93E  0B941                     TUQ  4F,0F
000E        0B941  0B942                    BICI  0L
000F        0B942  0B943  6R      0000       CPY  SP,6F
0010        0B942  0B943  6L  0D19
0011        0B943  0B944                     WPS  0L,6F
0012        0B944  0B945                     WBN  0; 5F
0013        0B945  0B946  7   0000B947       TPR  01,0F
0014        0B945  0B946
0015        0B946  0D492  0L  0000           TPR  7R
0016        0B946  0D492
0017        0D492  0B948                     TBZ  B948,2,SP
0018        0B948  0B948
0019        0B948  0B948
001A        0B948  0B948
001B        0B948  0B948
001C        0B948  0B948
001D        0B948  0B948
001E        0B948  0B948
001F        0B948  0B948
0020        0B948  0B948

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0000XXXX 0D14XXXX 8D140000 XXXXXXXX 00000000 00000000 0D190000 0000B947

** MONITOR ** V1.2
```

Figure 8. SMI Instruction Executed and Resulting Trace Dump.

00071

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=L
** MONITOR ** V1.2

I* RESTART

** MONITOR ** V1.2

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  0800  09EC4  0B936  4   00000000
0002        0B936  0B937  5   00000000
0003        0B937  0B938  4R      0000
0004        0B937  0B938  4L  0000
0005        0B938  0B939  5    0000000
0006        0B939  0B93A  4R      0000
0007        0B939  0B93A  4L  0000
0008        0B93A  0B93B  2R      0000
0009        0B93A  0B93B  2L  9195
000A        0B93B  0B93C  1L  1195
000B        0B93C  0B93D
000C        0B93D  0B93E
000D        0B93E  0B941
000E        0B941  0B942
000F        0B942  0B943  6R      0000
0010        0B942  0B943  6L  119A
0011        0B943  0B944
0012        0B944  0B945
0013        0B945  0B946  7   0000B947
0014        0B945  0B946
0015        0B946  0D492  0L  0000
0016        0B946  0D942
0017        0D492  0B948
0018        0B948  0B948
0019        0B948  0B948
001A        0B948  0B948
001B  *

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0000XXXX 1995XXXX 91950000 XXXXXXXX 00000000 00000000 119A0000 0000B947

** MONITOR ** V1.2
```

Figure 9. Edit Mode Loop Inhibit Feature.

00072

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=INS
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=028ED
EVENT CAPTURE (A,Q)=A
5 STOP(ADDR,EXT,OVFL)=OVFL
EVENTS=F
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA            SMI TRACED

0001  0800  028EC  028ED                         CHA  4R,4R
0002        028ED  0297F  0   00000000           XEC  4R
0003        028ED  0297F                         TPR  4L
0004        0297F  0294D  5L  0001               CHA  0F,5L
0005        0294D  0294E
0006        0294E  0294F  4L  0002
0007        0294F  02950
0008        02950  02951  7   0DB32952
0009        02950  02951
000A        02951  02795  7R      2953
000B        02795  02796  0L  0DC7
000C        02795  02796
000D        02796  02797  7   0DC72793
000E        02796  02797
000F        02797  03741

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0DC70000 XXXXXXXX XXXXXXXX XXXXXXXX 0002XXXX 0001XXXX XXXXXXXX 0DC72798

** MONITOR ** V1.2
```

Figure 10. Macroinstruction Trace Setup and Resulting Trace Dump.

```
I* MODIFY 4

4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=R028ED:0294F
EVENT CAPTURE (A,Q)=Q
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

I* STOP

** MONITOR ** V1.2

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  0006  028EC  028ED
0002        028ED  0297F   0  00000000
0003        028ED  0297F
0004        0297F  0294D  5L  0001
0005        0294D  0294E
0006        0294E  0294F  4L  0002

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
00000000 XXXXXXXX XXXXXXXX XXXXXXXX 0002XXXX 0001XXXX XXXXXXXX XXXXXXXX

** MONITOR ** V1.2
```

Figure 11. Modification of Previous Trace Example (Figure 10).

00074

```
I* MODIFY 4

4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=R028ED:0294F
EVENT CAPTURE (A,Q)=A
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  0800  028EC  028ED
0002        028ED  0297F  0   00000000
0003        038ED  0297F
0004        0297F  0294D  5L  0001
0005        0294D  0294E
0006        0294E  0294F  4L  0002
0007        0294F  02950
0008        02950  02951  7   0DB32952
0009        02950  02951
000A        02951  02795  7R      2953
000B        02795  02706  0L  0DC7
000C        02795  02796
000D        02796  02797  7   0DC72798
000E        02796  02797
000F        02797  03741
0010        03741  03742

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0DC70000 XXXXXXXX XXXXXXXX XXXXXXXX 0002XXXX 0001XXXX XXXXXXXX 0DC72798

** MONITOR ** V1.2
```

Figure 12. Modification of INS Trace Example (Figure 10).

00075

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=R
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=XFR
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=2988
EVENT CAPTURE (A,Q)=A
5 STOP(ADDR,EXT,OVFL)=ADDR
STOP ADDR=294D
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0DB30000 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX 0DB328E8

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  000E  0297F  0294D
0002        03747  028E8                Multiple Processor Operation
0003        03747  028E8  0L  0DB3
0004        028E7  03741                     "         "         "
0005        028E7  03741  7   0DB328E8
0006        029BF  028E6                     "         "         "
0007        209BF  028E6  7   0DAC29AB
0008        0299F  029A3
0009        02996  0299C
000A        0298D  02993
000B        07706  0298C
000C        0298B  07703
000D        04AF4  02988
000E        04AE4  02988  0   00000000       "         "         "

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
00000000 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX 0DAC29AB

** MONITOR ** V1.2
```

NOTE: The first register summary contains the latest known register contents within the limits of the trace buffer dump. The second register summary contains the oldest known register contents within the limits of the trace buffer dump.

Figure 13. INS Trace Modification of Previous Example (Figure 10).

00076

```
I* TRACE

**TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=IS
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR =R2795:2A27
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

I* STOP

** MONITOR ** V1.2

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0022  027A8  02A91     00202A6E  000 10
0002        027AB  02A91     00202A6E  000 10
0003        027B6  02A6E     2A010207  000 10
0004        027B6  02A6E     2A010207  000 10
0005        027B6  02A6E     2A010207  000 10
0006        027B6  02A6E     2A010207  000 10
0007        027B6  02A6F     04050607  000 10
0008        027B6  02A6F     04050607  000 10
0009        027B6  02A6F     04050607  000 10
000A        027B6  02A6F     04050607  000 10
000B        027B6  02A70     08090A0F  000 10
000C        027B6  02A70     08090A0F  000 10
000D        027B6  02A70     08090A0F  000 10
000E        027B6  02A70     08090A0F  000 10
000F        027B6  02A71     0C0D0E0F  000 10
0010        027B6  02A71     0C0D0E0F  000 10

** MONITOR ** V1.2
```

Figure 14. Progressive IS Trace for RIS of IS Memory.

00077

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=0
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=IS
READ-WRITE(R,W,B)=R
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=2A91
EVENT CAPTURE (A,Q)=A
DATA=
5 STOP(ADDR,EXT,OVFL)=ADDR
STOP ADDR=2A70
6 IAR =R27A8:27B6
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  000B  027A8  02A91     00202A6E  000 10
0002        027AB  02A91     00202A6E  000 10
0003        027B6  02A6E     2A010207  000 10
0004        027B6  02A6E     2A010207  000 10
0005        027B6  02A6E     2A010207  000 10
0006        027B6  02A6E     2A010207  000 10
0007        027B6  02A6F     04050607  000 10
0008        027B6  02A6F     04050607  000 10
0009        027B6  02A6F     04050607  000 10
000A        027B6  02A6F     04050607  000 10
000B        027B6  02A70     08090A0F  000 10

** MONITOR ** V1.2
```

Figure 15. IS Address of 2A91 for Trace Start Event and Address 2A70 for Stop Event.

00078

```
I* MODIFY 4

4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=2A91
EVENT CAPTURE (A,Q)=Q
DATA=
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.2

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0002  027A8  02A91     00202A6E  000 10
0002        027AB  02A91     00202A6E  000 10

** MONITOR ** V1.2
```

NOTE: This type of trace should be used when the IS address is known, and the IAR and the IS data contents are desired.

Figure 16. Modification of Previous Trace (Figure 15).

00079

```
I* MODIFY 4

4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=2A91
EVENT CAPTURE (A,Q)=A
DAT=00202A6E
MASK=
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

I* STOP

** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0022  027A8  02A91     00202A6E  000 10
0002        027AB  02A91     00202A6E  000 10
0003        027B6  02A6E     2A010207  000 10
0004        027B6  02A6E     2A010207  000 10
0005        027B6  02A6E     2A010207  000 10
0006        027B6  02A6E     2A010207  000 10
0007        027B6  02A6F     04050607  000 10
0008        027B6  02A6F     04050607  000 10
0009        027B6  02A6F     04050607  000 10
000A        027B6  02A6F     04050607  000 10
000B        027B6  02A70     08090A0F  000 10
000C        027B6  02A70     08090A0F  000 10
000D        027B6  02A70     08090A0F  000 10
000E        027B6  02A70     08090A0F  000 10
000F        027B6  02A71     0C0D0E0F  000 10
0010        027B6  02A71     0C0D0E0F  000 10

** MONITOR ** V1.1
```

Figure 17. IS Data Trace with Data Qualifications.

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=IS
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=X2A70:2A91
EVENT CAPTURE (A,Q)=Q
DATA=
5 STOP(ADDR,EXT,OVFL)=OVFL
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

I* STOP

** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0008  027B6  02A6E     2A010207  000 10
0002        027B6  02A6E     2A010207  000 10
0003        027B6  02A6E     2A010207  000 10
0004        027B6  02A6E     2A020207  000 10
0005        027B6  02A6F     04050607  000 10
0006        027B6  02A6F     04050607  000 10
0007        027B6  02A6F     04050607  000 10
0008        027B6  02A6F     04050607  000 10

** MONITOR ** V1.1
```

Figure 19. IS Trace with IS Outside Range.

00082

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=IS
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=R2A70:2A91
EVENT CAPTURE (A,Q)=Q
DATA=0809FFFF
MASK=0000FFFF
5 STOP(ADDR,EXT,OVFL)=OVFL
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0800   027B6  02A70     08090A0F  000 10
0002         027B6  02A70     08090A0F  000 10
0003         027B6  02A70     08090A0F  000 10
0004         027B6  02A70     08090A0F  000 10

** MONITOR ** V1.1
```

Figure 18. IS Trace with IS Inside Range and Data/Mask Qualifications.

00081

```
I* TRACE

** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=IS
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR =X2795:2A27
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

I* STOP

** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0286  04E94  00AB1     001F001F  000 10
0002        03306  00AB1     001F001F  000 10
0003        03702  03740     00000084  000 10
0004        04E94  00AB1     001F001F  000 10
0005        03306  00AB1     001F001F  000 10
0006        03702  03740     00000084  000 10
0007        04E94  00AB1     001F001F  000 10
0008        03306  00AB1     001F001F  000 10
0009        03702  03740     00000084  000 10
000A        04E94  00AB1     001F001F  000 10
000B        03306  00AB1     001F001F  000 10
000C        03702  03740     00000084  000 10
000D        04E94  00AB1     001F001F  000 10
000E        03306  00AB1     001F001F  000 10
000F        03702  03740     00000084  000 10
0010        04E94  00AB1     001F001F  000 10

** MONITOR ** V1.1
```

Figure 20. IS Data Trace with IAR Outside Range.

00083

```
I* TRACE

** TRACE **
1 COPY(O,1,B)=1
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=PS
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR= R294D;2952
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

I* STOP

** MONITOR ** V1.2

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0002  0294E  01DB4     00010000  100 01
0002        02950  01DB5     00020008  100 01

** MONITOR ** V1.1
```

Figure 21. PS Data Trace with IAR Inside Range.

```
** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=MEM
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=R20000:22000
EVENT CAPTURE (A,Q)=A
DATA=
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR=
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP      SMI

0001  0800   0661F  2190B     190B190B  000 01    READ PS   RPS
0002         06621  2190B     190B190B  000 01    READ PS   RPS
0003         06623  2190B     190B190B  000 01    READ PS   RPS
0004         06624  0662F     5F686618  010 10    FETCH IS  TEH
0005         0662F  06618     A7881000  010 10    FETCH IS  TEH
0006         06618  01005     000044E2  000 01    READ PS   RPS
0007         0661A  01005     000044E1  100 01    WRITE PS  WPS
0008         0661B  0360F     A6880FFD  010 10    FETCH IS  TPR
0009         0360F  01002     00000000  000 01
000A         03610  01003     11740000  000 01
000B         03611  01004     00510004  000 01
000C         03612  01005     000044E1  000 01
000D         03613  044E1     600044F1  010 10
000E         044E1  044F1     224C0001  010 10
000F         044F3  044DE     5E4444E8  010 10
0010         044DE  044E8     B6002846  010 10

** MONITOR ** V1.1
```

Figure 22. MEM Data Trace with Start Address Inside Range.

00085

```
** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=PC
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR=R3399:333B
EVENTS=10
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1


LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0800  03308  0001F     00000000  001 00    PAU READ
0002        03310  0001F     00000001  101 00    PAU WRITE
0003        03311  0001F     00000001  001 00
0004        03310  0001F     00000002  101 00
0005        03311  0001F     00000002  001 00
0006        03310  0001F     00000004  101 00
0007        03311  0001F     00000004  001 00
0008        03310  0001F     00000008  101 00
0009        03311  0001F     00000008  001 00
000A        03310  0001F     00000010  101 00
000B        03311  0001F     00000010  001 00
000C        03310  0001F     00000020  101 00
000D        03311  0001F     00000020  001 00
000E        03310  0001F     00000040  101 00
000F        03311  0001F     00000040  001 00
0010        03310  0001F     00000080  101 00


** MONITOR ** V1.1
```

Figure 23. PC Data Trace.

```
** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=CMD
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=CMD
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR =R3300:3320
EVENTS=30
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1
```

LINE	EVENTS	IAR	R/W-ADR	DATA	OP TYPE		SMI
0001	0800	03300	03304	62803304	011 10	PIPELINE FETCH IS	WSI
0002		03300	0100B	E209100B	100 01	WRITE PS	
0003		03301	02E4E	00002E4E	110 00	WRITE DATA	TPR
0004		03301	03741	62803741	010 10	FETCH IS	
0005		03301	03742	62803742	011 10	PIPELINE FETCH IS	
0006		03301	03743	62803743	011 10	PIPELINE FETCH IS	
0007		03301	03744	62803744	011 10	PIPELINE FETCH IS	
0008		03302	01A00	62801A00	010 10	FETCH IS	TPR
0009		03302	01A01	62801A01	011 10	PIPELINE FETCH IS	
000A		03302	01A02	62801A02	011 10	PIPELINE FETCH IS	
000B		03302	01A03	62801A03	011 10	PIPELINE FETCH IS	
000C		03304	03306	62803306	010 10	FETCH IS	TBN
000D		03304	03307	62803307	011 10	PIPELINE FETCH IS	
000E		03304	03308	62803308	011 10	PIPELINE FETCH IS	
000F		03304	03309	62803309	011 10	PIPELINE FETCH IS	
0010		03306	00AB1	62800AB1	000 10	READ IS	RIS
0011		03306	0330A	6280330A	011 10	PIPELINE FETCH IS	
0012		03307	0030B	6280330B	011 10	PIPELINE FETCH IS	
0013		03308	0330C	6280330C	011 10	PIPELINE FETCH IS	
0014		03308	0001F	C388001F	001 00	READY PAU	
0015		03308	060FF	C15F60FF	010 00	RETURN PAU (ECHO)	
0016		0330A	0330D	6280330D	011 10	PIPELINE FETCH IS	CPH
0017		0330A	0330E	6280330E	011 10	PIPELINE FETCH IS	
0018		0330A	00105	00000105	110 00	WRITE DATA	
0019		0330A	00000	C15F0000	101 00	RETURN PAU (ECHO)	
001A		0330B	01003	E2091003	100 01	WRITE PS	WPS
001B		0330C	00000	00000000	110 00	WRITE DATA	CPH
001C		0330D	0330F	6280330F	011 10	PIPELINE FETCH IS	CPH
001D		0330E	03310	62803310	011 10	PIPELINE FETCH IS	CPH
001E		0330E	03311	62803311	011 10	PIPELINE FETCH IS	
001F		0330E	03312	62803312	011 10	PIPELINE FETCH IS	
0020		0330F	01004	E2091004	100 01	WRITE PS	WPS
0021		03310	0001F	001F001F	110 00	WRITE DATA	WPU
0022		03310	03313	62803313	011 10	PIPELINE FETCH IS	
0023		03310	0001F	C348001F	101 00	WRITE PAU	
0024		03310	00001	00000001	110 00	WRITE DATA	

Figure 24. Command Bus (CMD) Trace (Sheet 1 of 2).

00087

```
0025        03310  03314     62803314  011 10    PIPELINE FETCH IS
0026        03310  060C8     C1BF60C8  010 00    RETURN PAU (ECHO)
0027        03311  03315     62803315  011 10    PIPELINE FETCH IS   RPU
0028        03311  03316     C2FF3316  111 11    REFRESH
0029        03311  03311     62803311  010 10    FETCH IS
002A        03311  00000     C1BF0000  010 00    RETURN PAU (ECHO)
002B        03311  03312     62803312  011 10    PIPELINE FETCH IS
002C        03311  03313     62803313  011 10    PIPELINE FETCH IS
002D        03311  0001F     C388001F  001 00    READ PAU (ECHO)
002E        03311  03314     62803314  011 10    PIPELINE FETCH IS
002F        03311  03315     62803315  011 10    PIPELINE FETCH IS
0030        03311  060FF     C15F60FF  010 00    PAU RETURN (ECHO)

** MONITOR ** V1.1
```

Figure 24. Command Bus (CMD) Trace (Sheet 2 of 2).

00088

```
I* DUMP 2D:40

LINE EVENTS IAR   R/W-ADR  DATA      OP TYP   PIPELINE FETCH IS   SMI

002D  0800  03311  03315    E2803315  011 10   PIPELINE FETCH IS   RPU
002E        03311  0001F    C388001F  001 00   PAU READ
002F        03311  060FF    C15F60FF  010 00   PAU RETURN (ECHO)
0030        03313  03316    E2803316  011 10   PIPELINE FETCH IS   CPH
0031        03313  03317    E2803317  011 10   PIPELINE FETCH IS
0032        03313  00000    C1BF0000  010 00   PAU RETURN
0033        03314  03318    C2FF3318  111 11   REFRESH             TEQ
0034        03314  03318    E2803318  011 10   PIPELINE FETCH IS
0035        03314  03318    E2803318  010 10   FETCH IS
0036        03314  03319    E2803319  011 10   PIPELINE FETCH IS
0037        03314  0331A    E280331A  011 10   PIPELINE FETCH IS
0038        03314  0331B    E280331B  011 10   PIPELINE FETCH IS
0039        03318  0331C    E280331C  011 10   PIPELINE FETCH IS   CRL
003A        03319  01004    E2891004  000 01   READ PS             RPS
003B        03319  0331D    E280331D  011 10   PIPELINE FETCH IS
003C        0331B  0330F    E280330F  010 10   FETCH IS            TIX
003D        0331B  03310    E2803310  011 10   PIPELINE FETCH IS
003E        0331B  03311    E2803311  011 10   PIPELINE FETCH IS
003F        0331B  03312    E2803312  011 10   PIPELINE FETCH IS
0040        0330F  01004    E2091004  100 01   WRITE PS            WPS

** MONITOR ** V1.1
```

Figure 25. CMD Trace with Buffer Dump Request.

00089

```
** TRACE **
1 COPY(0,1,B)=0
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=DMA
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR=
EVENTS=20
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP
0001  0800  0330B  11B80     A4960280  101 01
0002        0330B  11B81     654002B0  101 01
0003        0330B  11B82     238002C0  101 01
0004        0330B  11B83     726802D0  101 01
0005        0330B  11B84     A4960280  101 01
0006        0330B  11B85     754002E0  101 01
0007        0330B  11B86     1E0002F0  101 01
0008        0330B  11B87     3CA00290  101 01
0009        0330B  11B88     625C5010  101 01
000A        0330B  11B89     24000450  101 01
000B        0330B  11B8A     24C61370  101 01
000C        0330B  11B8B     24C62380  101 01
000D        0330B  11B8C     25000460  101 01
000E        0330B  11B8D     28A403E0  101 01
000F        0330B  11B8E     28A53400  101 01
0010        0330B  11B8F     28A603F0  101 01
0011        0330B  11B90     28A72400  101 01
0012        0330B  11B91     61240440  101 01
0013        0330B  11B92     64C60620  101 01
0014        0330B  11B93     65280490  101 01
0015        0330B  11B94     6C8004C0  101 01
0016        0330B  11B95     7144D3D0  101 01
0017        0330B  11B96     726801E0  101 01
0018        0330B  11B97     73092430  101 01
0019        0330B  11B98     736404B0  101 01
001A        0030B  11B99     74D94580  101 01
001B        0330B  11B9A     74E54550  101 01
001C        0330B  11B9B     74EC34A0  101 01
001D        0330B  11B9C     769E9600  101 01
001E        0330B  11B9D     9B280590  101 01
001F        0330B  11B9E     9CA80560  101 01
0020        0330B  11B9F     9D860A80  101 01

** MONITOR ** V1.1
```

Figure 26. DMA Data Trace.

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=A
ADDR(IAR,RW)=RW
ADDR=11B94
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP
0015  0800  0300B  11B94     6C8004C0  101 01

** MONITOR ** V1.1
```

Figure 27. Read/Write Address Edit.

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=A
ADDR(IAR,RW)=RW
ADDR=R11B96:11B9C
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0017  0800  0330B  11B96     726801E0  101 01
0018        0330B  11B97     73092430  101 01
0019        0330B  11B98     73640480  101 01
001A        0030B  11B99     74D94580  101 01
001B        0330B  11B9A     74E54550  101 01
001C        0330B  11B9B     74EC34A0  101 01
001D        0330B  11B9C     769E9600  101 01

** MONITOR ** V1.1
```

Figure 28. Read/Write Address Inside Range Edit.

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=A
ADDR(IAR,RW)=RW
ADDR=X11B83:11B94
** MONITOR ** V1.1

I* DUMP 1:20

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0800  0330B  11B80     A4960280  101 01
0002        0330B  11B81     654002B0  101 01
0003        0330B  11B82     238002C0  101 01
0016        0330B  11B95     7144D3D0  101 01
0017        0330B  11B96     726801E0  101 01
0018        0330B  11B97     73092430  101 01
0019        0330B  11B98     736404B0  101 01
001A        0330B  11B99     74D94580  101 01
001B        0330B  11B9A     74E54550  101 01
001C        0330B  11B9B     74EC34A0  101 01
001D        0330B  11B9C     769E960C  101 01
001E        0330B  11B9D     98280590  101 01
001F        0330B  11B9E     9CA80560  101 01
0020        0330B  11B9F     9D860A80  101 01

** MONITOR ** V1.1
```

Figure 29. Edit.

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=D
DATA=73092430
MASK=
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0018  0800  0330B  11B97     73092430  101 01
0237        0330B  11DB6     73092430  101 01

** MONITOR ** V1.1
```

Figure 30. Data Edit.

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=D
DATA=80
MASK=FFFFFF0F
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0800  0330B  11B80     A4960280  101 01
0005        0330B  11B84     A4960280  101 01
000C        0330B  11B8B     24C62380  101 01
001A        0330B  11B99     74D94580  101 01
0020        0330B  11B9F     9D860A80  101 01
0029        0330B  11BA8     19121680  101 01
0043        0330B  11BC2     9B428780  101 01
004B        0330B  11BCA     9BE80280  101 01
007E        0330B  11BFD     1CE80280  101 01
007F        0330B  11BFE     1CF13080  101 01

I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=D
DATA=1BE80000
MASK=FFFF
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0292  0800  0330B  11E11     1BE80365  101 01
0293        0330B  11E12     1BE82683  101 01
0294        0330B  11E13     1BE81A79  101 01
0298        0330B  11E17     1BE8121D  101 01
029A        0330B  11E19     1BE81650  101 01
029D        0330B  11E1C     1BE8249F  101 01
029F        0330B  11E1E     1BE86150  101 01
02A1        0330B  11E20     1BE8121D  101 01
02A5        0330B  11E24     1BE800AD  101 01
02A6        0330B  11E25     1BE800AD  101 01
02A7        0330B  11E26     1BE800AD  101 01
02A9        0330B  11E28     1BE800AD  101 01
```

Figure 31. Data/Mask Edit (Sheet 1 of 2).

02AA	0330B	11E29	1BE81A79	101 01
02AB	0330B	11E2A	1BE81A79	101 01
02AC	0330B	11E2C	1BE800AD	101 01
02AD	0330B	11E2C	1BE800AD	101 01
02AE	0300B	11E2D	1BE8121D	101 01
02AF	0330B	11E2E	1BE81A79	101 01
0252	0330B	11E31	1BE8249E	101 01

Figure 31. Data/Mask Edit (Sheet 2 of 2).

```
** TRACE **
1 COPY(0,1,B)=0
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=INS
4 START(ADDR,EXT,IMMED)=ADDR
START ADDR=B936
EVENT CAPTURE (A,0)=A
5 STOP(ADDR,EXT,OVFL)=OVFL
EVENTS=20
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  0800  09EC4  0B936  4   00000000
0002        0B936  0B937  5   00000000
0003        0B937  0B938  4R      0000
0004        0B937  0B938  4L  0000
0005        oB938  0B939  5   00000000
0006        0B939  0B93A  4R      0000
0007        0B939  0B93A  4L  0000
0008        0B93A  9B93B  2R      0000
0009        0B93A  0B93B  2L  8E62
000A        0B93B  9B93C  1L  0E62
000B        0B93C  9B93D
000C        0B93D  0B93E
000D        0B93E  0B941
000E        0B941  0B942
000F        0B942  0B943  6R      0000
0010        0B942  0B943  6L  0E67
0011        0B943  0B944
0012        0B944  0B945
0013        0B945  0B946  7   0000B947
0014        0B945  0B946
0015        0B946  0D492  0L  0000

I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=R
GR=4
** MONITOR ** V1.1

I* RESTART

** MONITOR ** V1.1
```

Figure 32. General Register Edit (Sheet 1 of 2).

```
LINE EVENTS FR-ADR TO-ADR GR  GR-DATA

0001  0800  09EC4  0B936  4   00000000
0003        0B937  0B938  4R      0000
0004        0B937  0B938  4L  0000
0006        0B939  0B93A  4R      0000
0007        0B939  0B93A  4L  0000

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
0000XXXX 0E3DXXXX 8E3D0000 XXXXXXXX 00000000 00000000 0E420000 0000B947

** MONITOR ** V1.1
```

Figure 32. General Register Edit (Sheet 2 of 2).

```
I* TRACE

** TRACE **
1 COPY(O,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=CMD
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR=R3300:3330
EVENTS=20
READY(Y,N,E,X,A)=E
** EDIT MODE **
EDIT(L,D,A,R,N)=N
** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0800  03300  03304     E2803304  011 10
0002        03300  0100B     E209100B  100 01
0003        03301  02E4E     00002E4E  110 00
0004        03301  03741     E2803741  010 10
0005        03301  03742     E2803742  011 10
0006        03301  03743     E2803743  011 10
0007        03301  03744     E2803744  011 10
0008        03302  01A00     E2801A00  010 10
0009        03302  01A01     E2801A01  011 10
000A        03302  01A02     E2801A02  011 10
000B        03302  01A03     E2801A03  011 10
000C        03304  03306     E2803306  010 10
000D        03304  03307     E2803307  011 10
000E        03304  03308     E2803308  011 10
000F        03304  03309     E2803309  011 10
0010        03306  00AB1     E2800AB1  000 10
0011        03306  0330A     E280330A  011 10
0012        03308  0330B     E280330B  011 10
0014        03308  0001F     C388001F  001 00
0015        03308  060FF     C1BF60FF  010 00

I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=A
ADDR(IAR,RW)=IAR
ADDR=3308
** MONITOR ** V1.1

I* RESTART
```

Figure 33. IAR Address Edit (Sheet 1 of 2).

```
** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0012  0800  03308  0330B     E280330B  011 10
0013        03308  0330C     E280330C  011 10
0014        03308  0001F     C388001F  001 00
0015        03308  060FF     C1BF60FF  010 00

** MONITOR ** V1.1
```

Figure 33. IAR Address Edit (Sheet 2 of 2).

```
** EDIT MODE **
EDIT(L,D,A,R,N)=A
ADDR(IAR,RW)=IAR
ADDR=R3311:3312
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0028  0800  03311  03315     E2803315  011 10
0029        03311  03311     E2803311  010 10
002A        03311  03312     E2803312  011 10
002B        03311  03313     E2803313  011 10
002C        03311  00000     C1BF0000  010 00
002D        03311  03314     E2803314  011 10
002E        03311  03315     E2803315  011 10
002F        03311  0001F     C388001F  001 00
0030        03311  060FF     C1BF60FF  010 00
0047        03311  03315     E2803315  011 10
0048        03311  03311     E2803311  010 10
0049        03311  03312     E2803312  011 10
004A        03311  03313     E2803313  011 10
004B        03311  00000     C1BF0000  010 00
004C        03311  03314     E2803314  011 10
004D        03311  03315     E2803315  011 10
004E        03311  0001F     C388001F  001 00
004F        03311  060FF     C1BF60FF  010 00
```

Figure 34. IAR Address Inside Range Edit.

00101

```
I* EDIT

** EDIT MODE **
EDIT(L,D,A,R,N)=A
ADDR(IAR,RW)=IAR
ADDR=X3305:3330
** MONITOR ** V1.1

I* DUMP 1:800

LINE EVENTS IAR    R/W-ADR   DATA      OP TYP

0001  0800  03300  03304     E2803304  011 10
0002        03300  0100B     E209100B  100 01
0003        03301  02E4E     00002E4E  110 00
0004        03301  03741     E2803741  010 10
0005        03301  03742     E2803742  011 10
0006        03301  03743     E2803743  011 10
0007        03301  03744     E2803744  011 10
0008        03302  01A00     E2801A00  010 10
0009        03302  01A02     E2801A02  011 10
000A        03302  01A02     E2801A02  011 10
000B        03302  01A03     E2801A03  011 10
000C        03304  03306     E2803306  010 10
000D        03304  03307     E2803307  011 10
000E        03304  03308     E2803308  011 10
```

Figure 35. IAR Address Outside Range Edit.

00102

```
** TRACE **
1 COPY(0,1,B)=B
2 MODE(P,R)=P
3 TYPE(IS,PS,PC,INS,XFR,MEM,DMA,CMD)=IS
READ-WRITE(R,W,B)=B
4 START(ADDR,EXT,IMMED)=IMMED
5 STOP(ADDR,EXT,OVFL)=OVFL
6 IAR=
EVENTS=10
READY(Y,N,E,X,A)=HITS
READY(Y,N,E,X,A)=Y
** MONITOR ** V1.1

I* HITS

00AC

** MONITOR ** V1.1

I* HITS

0189
** MONITOR ** V1.1

I* HITS

02CF
** MONITOR ** V1.1

I* STOP

** MONITOR ** V1.1

LINE EVENTS IAR    R/W-ADR  DATA     OP TYP
0001  0370  03306  00AB1    001F001F 000 10
0002        03702  03740    00000080 000 10
0003        04E94  00AB1    001F001F 000 10
0004        03306  00AB1    001F001F 000 10
0005        03702  03740    00000080 000 10
0006        04F94  00AB1    001F001F 000 10
0007        03306  00AB1    001F001F 000 10
0008        03702  03740    00000080 000 10
0009        04E94  00AB1    001F001F 000 10
000A        03306  00AB1    001F001F 000 10
000B        03702  03740    00000080 000 10
000C        04E94  00AB1    001F001F 000 10
000D        03306  00AB1    001F001F 000 10
000E        03702  03740    00000080 000 10
000F        04E94  00AB1    001F001F 000 10
0010        03306  00AB1    001F001F 000 10

** MONITOR ** V1.1
```

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TYPE 2B PROCESSOR COMPLEX
X-RAY PROGRAMS
DESCRIPTION AND USE

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00107

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00108

1. GENERAL

1.01 This section provides a functional description and user's guide information for the Type 2B Processor Complex X-ray (microdiagnostic) programs.

1.02 The X-ray programs are used during the initial installation of a Type 2B Processor Complex Control and Memory Complex (CMC) to provide basic system integrity in a simplex configuration such that system software (macro) diagnostics can be loaded from a system magnetic tape (initial program load). The system diagnostics are then used to bring up a full-triplex CMC configuration and to perform more comprehensive diagnostics on a system level.

1.03 For a functional description of the Type 2B Processor Complex, refer to Section 227-200-100.

2. PREREQUISITES

2.01 Before attempting to use the information in this section, the user should be familiar with the following documents:

(a) Section 227-200-300, Type 2B Processor Complex System Monitor - Description and Use.

(b) Section 227-201-502, Type 2B Processor Complex System Monitor - Static and Dynamic Installation Test Procedure.

2.02 The user should also obtain a set of X-ray assembler listings to complement the information in this section, and to aid in troubleshooting hardware problems.

3. DESCRIPTION

3.01 The X-ray program is generated in Type 2B Processor Complex firmware microcode as an object file output from the micro-assembler resident on magnetic disk. A utility program (X-Ray2) is used to transfer the exact image of the object file (binary form) from the minicomputer to a floppy-disk file. The data is then verified by reading it back from the floppy disk and comparing it word-by-word with the original binary file. Another utility program is used

to read the object file from floppy disk, reorder the data, and write it to a tape cartridge on the system monitor. The data is then reread from the floppy disk and tape cartridge and compared.

3.02 Before the data is written on the tape cartridge, a tape header is manually entered at the system monitor terminal and written on the tape. There must be one tape cartridge for each X-ray program generated.

3.03 The X-ray programs are loaded into the system monitor Read-Only Memory Simulator (ROMSIM) from the magnetic tape cartridge using the system monitor X-ray commands. The ROMSIM (1K, where K=1,024, Random Access Memory (RAM)) is physically attached to one of the three Central Processors (CP's) within the CMC. The chosen CP is forced master by a backplane strap that also disables the other two CP's. Refer to Section 227-201-502 for detailed information.

3.04 When entered manually from the system monitor terminal, X-ray commands enable the ROMSIM (which disables the central processor's Control ROM (CROM). As the CP performs actions directed by the X-ray micro-instructions, the system monitor captures data in its trace memory. The captured data may then be manually analyzed to determine if the X-ray program(s) were executed correctly. The type of information to be captured during X-ray execution is established using the system monitor trace control commands. Refer to Section 227-200-300 for detailed information.

3.05 After an X-ray program has been loaded, the trace set up, and the execution started, the operator can use system monitor trace control commands to stop data capture, change the type of information being captured, edit the data already captured, or restart the trace data capture. While the operator is making system monitor trace control changes, the X-ray program will continue running and will only be stopped if the X-ray control mode is re-entered. Thus, it is not necessary to reload a tape cartridge each time the system

monitor trace parameters are changed; it is only necessary to reload if a new X-ray is to be executed.

3.06 When the X-ray control mode is entered, the CP under test is stopped. When the X-ray execution command is given, the CP's microprogram counter is forced to location 0 and micro-instruction code is then executed on a CP run signal from the system monitor.

X-Ray Program Structure

3.07 All X-ray programs have dedicated microlocations and are designed to operate within 1K words of ROMSIM memory. The starting micro-address must always be location 0. Refer to Figure 1 for X-ray program (ROMSIM) locations.

3.08 Microlocations 0 through 4 are reserved for startup procedures, and locations 5 through 7 are reserved for trace capture stop addresses. Locations 8 and 9 are used for the sequence control table (for operator control), and locations 300 through 3FF are used for the parameter control table (also for operator control). All X-ray programs are subdivided into independent phases, the number and functions of which are dependent upon the given program. The operator determines which particular phase(s) of a given program are executed; this is accomplished by means of X-ray control commands for the sequence control table.

3.09 All X-ray programs transfer to microlocation 5 upon completion of all (or specified) phases. If no error was detected during program execution, the programs transfer to location 7 first, and then to location 5 before restarting execution. If an error was detected, the programs transfer to location 6 first, and then to location 5 before restarting execution.

3.10 General Registers (GR's) 0 through 7 are used for X-ray tracing of phase identification and error information. This is because the system monitor can

only capture the A-file lower register (GR0 through GR7). Registers 9 through 15 of the A-file, and all of the B-file registers are used as internal working GR's by the X-ray programs, and are not capturable by the system monitor. There is a correlation between GR's and X-ray program structure in that if no error is encountered during program execution and the program transfers to location 7, GR0 is the only register that contains meaningful data. If an error is encountered during program execution and the program transfers to location 6, all useful error data is contained in GR0 through GR7.

3.11 For an illustration of standard GR formats, refer to Figure 2. The data contained in the GR's is as follows:

(a) GR0. The particular X-ray program number, interval phase number of test (0 to 15, depending upon the program), and unique fault-identification number.

(b) GR1. Collection of internal CP indicates.

(c) GR2. Refer to Figure 3. Expected test values (for specific X-ray program operations) that are compared to the actual value received.

(d) GR3. Actual test values received (as a result of specific X-ray program operations) that are compared to expected test values.

(e) GR4. Run count incremented for each X-ray program run and error count incremented for each error encountered. Both the run count and the error count are reset by AUTORESTART occurrence and X-ray command E.

(f) GR5, GR6, and GR7. The definition and format of these GR's are dependent upon and vary according to the requirements of each X-ray program.

Normal X-Ray Trace Setup

3.12 In order to trace X-ray programs, it is necessary to specify a regressive (last in, first out) instruction trace. The start event should be immediate and the stop event should be address 5. The example shown in Figure 4 should be used as a typical trace setup for all X-ray programs.

Special X-Ray Trace Setup

3.13 It may be necessary to use a trace setup other than the normal setup (Figure 4) to trace hardware-unique problems. The specified instruction trace type should be adequate for most cases, but any other trace type can be used. However, certain precautions must be taken or the resultant data may be irrelevant to tracing the problem under investigation, and possibly erroneous.

3.14 Refer to Section 227-200-300 for detailed information on the desired trace setup. Some desirable setups may be to use a progressive trace on only one of the bus copies for either memory or command bus trace types qualified by a read/write or IAR address, and to edit the trace buffer dump for a particular address or data pattern.

X-Ray Loading

3.15 The selected X-ray program magnetic tape cartridge is inserted into the magnetic cartridge tape drive assembly. If the system is not already in the X-ray mode, input the following:

```
I*<X-RAY>
**X-RAY**
```

Then enter the X-ray command to load the tape into the ROMSIM, as follows:

```
X-RAY (S,L,E,EM,I,T,P,C) = <L>
**CARTRIDGE IN OK -- REWINDING**
X-RAY NAME, DATE, VERSION
**VERIFY STARTED**
II VERIFY COMPLETE**
```

Normal Program Execution

3.16 If no modifications are to be made to either the sequence control or parameter control tables, ensure that the desired CP is master by inputting the following:

```
X-RAY (S,L,E,EM,I,T,P,C) = <E>
```

Special Program Execution

3.17 At times, it may be necessary to use other than the normal X-ray execution, which captures on those microlocations in which modifications are made to any of the GR's. The following X-ray command feature allows the tracing of all addresses executed:

I*<X-RAY>

X-RAY

X-RAY (S,L,E,EM,I,T,P,C) =

ADDRESS TYPE (MICRO, MACRO) = <MICRO>

MICRO ADDR EVENT (FORCE, REF) = <FORCE>

3.18 Care must be taken in the analysis of this type of trace, because the system monitor can only capture the instruction at the CP decode taken signal. If the instruction being executed contains a conditionality, the CP normally increments the microprogram counter at decode and then tests the conditionality of the instruction. Therefore, the trace contains both address conditions of the instruction, and analysis of the program code is required for correct intepretation of trace data.

Program Execution Sequence

3.19 To use a simplex CP to test itself and to verify a simplex path to the system magnetic tape unit, the X-ray programs should be executed successfully in the order specified in Table 1. The programs listed in Table 1 are designed to verify basic CMC sanity and are not intended for extensive nor complete problem diagnosis. For more information on these programs, refer to part 4.

4. USE

4.01 This part provides more detailed information on the X-ray programs listed in Table 1.

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Instruction Sequence Test (SEQTST)

4.02 The SEQTST (version B01) program tests and verifies the basic micro-instructions and address sequencing of the CP. This test should be the first X-ray program executed for initial bringup. Any faults encountered should be corrected before progressing to the next test.

4.03 For initial bringup, the sanity of the CP is unknown. For this reason, the SEQTST does not include phase select or parameter control tables that require more complex microinstruction execution. The type of microinstructions verified by the SEQTST program are as follows:

(a) GOTO

(b) NOP

(c) SKIP

(d) SKIP IF NOT TRUE

(e) SKIP IF NOT ZERO

(f) SKIP IF TRUE

(g) EXEC

(h) NESTED CALL-RETURN

(i) A FILE GENERAL REGISTER 0-7 DATA

4.04 A typical SEQTST trace setup and execution is shown in Figure 5. If a fault occurs in the basic GOTO tests, it will be necessary for the operator to set up a progressive in-service trace with the start event being micro address 4, and the X-ray execution on Execute Modify (EM), (MICRO) address, and FORCE every sequenced microlocation. Refer to paragraphs 3.17 and 3.18 for more information.

4.05 The error displays shown in Figure 6 are valid if the X-ray execution with a normal trace setup fails (FR-ADDR = 00006, TO-ADDR = 00005).

Main Data Structure Test (ALUTST)

4.06 The ALUTST (version B03) program tests and verifies the basic data structure of the CP. There are 14 phases (0 through E) in this test program. The ALUTST phases and their functions are listed in Table 2. The normal X-ray program trace setup (Figure 4) should be used for the ALUTST.

4.07 The phase selection associated with this program allows a variable start phase. However, it does not allow the running of an individual phase only. The normal execution mode should be used for the ALUTST (Figure 7).

4.08 If the program encounters an error during execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 8 are valid.

Clock Test (CLKTST)

4.09 The CLKTST (version B01) program tests the basic clock logic for setting and/or resetting clock errors and switching clocks. There are no phase select or parameter control tables associated with the CLKTST program. For a typical CLKTST trace setup and execution, refer to Figure 9.

4.10 If the program encounters an error during execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 10 are valid.

Test Point Test (TTEST)

4.11 The TTEST (version B53) program tests and verifies proper operation of the Central Processor Unit (CPU) internal multiple test selection logic. There are no phase select or parameter control tables associated with the TTEST program. The TTEST program performs the following two tests:

(a) Pointer test.

(b) Special error test.

4.12 For the pointer test, the program first resets all errors and then individually tests the status of each of the 29 test points. Upon completion of the test, the status of the test points is displayed in REGOL-7L.

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4.13 The normal X-ray program trace setup (Figure 4) should be used for the TTEST program.

4.14 The register display shown in Figure 11 should be examined upon completion of the test, regardless of the pass/fail condition. Any abnormal condition indicates an error. If the program encounters an error during execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 12 are valid.

Basic Bus Test (BUSTST)

4.15 The BUSTST (version B62) program tests and verifies proper operation of various CP timers, counters, initial program load ROM, and the basic bus operations to the Bus Interface Unit (BIU). The program provides nine tests, some of which include various phases. A listing of the tests and phases of each test is provided in Table 3. Descriptions of the tests and phases are provided in paragraphs 4.16 through 4.25.

4.16 Test 0 - Manual Access Point (MAP) Test. This test verifies the basic operations of addressing, writing, and reading the MAP memory address translation contained on BCTL-2 (card FB-15648). The phases of test 0 are as follows:

(a) Phase 1. Verifies MAP writes to the 32 addresses using all the even data bits.

(b) Phase 2. Verifies MAP reads to the 32 addresses using all the even data bits.

(c) Phase 3. Verifies MAP writes to the 32 addresses using all the odd data bits.

(d) Phase 4. Verifies MAP reads to the 32 addresses using all the odd data bits.

(e) Phase 5-1F. Verifies data pattern writes and reads to all 32 MAP addresses.

4.17 Test 1 - Special Purpose Register (SPR) timer test. This test verifies the basic operation of the SPR timer by:

(a) Stopping and clearing the SPR and checking to ensure that the SPR count is 0.

(b) Waiting for 16 clocks and ensuring that SPR is 0.

(c) Clearing the decode counter and enabling the SPR 2 microsecond count, then ensuring that the SPR time-out is reset.

(d) Checking SPR count and SPR time-out.

(e) Resetting SPR time-out and SPR to 0.

4.18 Test 2 - Utility Counter Test. This test verifies the basic operation of the utility counter by:

(a) Clearing the counter and ensuring that it does not indicate a negative value (CNTRM1), and that it does indicate 0.

(b) Starting the counter, and, while it is counting, ensuring that it does not initially indicate negative, equals the correct count, and eventually equals 0.

4.19 Test 3 - Refresh Timer Test. This test verifies the basic operation of the refresh timer by ensuring that the refresh period is neither too short nor too long. It ensures that the refresh flag is reset at the proper time. It also uses the bus history stack to verify proper bus commands/data for a refresh operation.

4.20 Test 4 - PAU Timer Test. This test verifies the basic operation of the Peripheral Access Unit (PAU) timer by ensuring that the timer can be reset without indicating a time-out, and by timing the operation of the timer for a time-out (2.6 microseconds). It also ensures that the PAU timer time-out flag and timer can be reset and restarted, and that a reset of the timer does reset the time-out flag.

00119

"CCCCCCCC"

"0F0F0F0F"

"F0F0F0F0"

"00FF00FF"

"FF00FF00"

"0000FFFF"

"FFFF0000"

4.22 Test 6 - IPL L Test. This test verifies the left Initial Program Load (IPL) ROM (bits 0 to 15) by means of a CRC check with the expected checksum being an operator-controlled parameter (issue 1 = "CE4C").

4.23 Test 7 - IPL R Test. This test verifies the right initial program load ROM (bits 16 to 31) by means of a CRC check with the expected checksum being an operator-controlled parameter (issue 1 = "B1D0").

4.24 The normal X-ray program trace setup (Figure 4) should be used for the BUSTST program.

4.25 Test 8 - Bus History Stack Test. An initial test is made to verify the basic operation of the bus history pointer load and spill functions. Then the following phase tests are performed:

(a) Phase 1. A test is made to verify the proper operation of the pointer decrementing.

(b) Phase 2. A test is made to verify the proper operation of the pointer freezing.

(c) Phase 3 - A functional test is made to verify the proper operation of the bus history stack, and checks are made for bus history data mismatch and spill information.

4.26 The BUSTST parameter control table contains the program information for the bus configuration and IPL tests. The bus configuration parameters determine

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the first configuration to be verified. The format is as shown in Figure 14a. (The program default parameter is 0000.) The IPL parameters (Figure 14b) determine the expected final checksum for the IPL CRC tests. The default parameters are set up for issue 1 initial program load ROM's and should be valid until an issue change occurs.

4.27 A typical BUSTST test selection and execution is shown in Figure 15.

Command-Response Bus Test (CRBTST)

4.28 The CRBTST (version B25) program verifies the basic operation of the system's command and response buses by writing and reading selected test patterns to MIU 0. The test consists of testing command buses 0 and 1 first, and response bus 0 for a ripple test and a checkboard test. The test is then repeated for response bus 1. The Processor Control and Display Console (PCDC) displays CRB to identify the CRBTST program.

4.29 The following steps are performed for the ripple test:

(a) Write/read all 0's with even parity.

(b) Write/read all 0's with flipper.

(c) Write/read a ripple 1 from right to left.

4.30 For the checkboard test, the following patterns are written/read in the sequence shown:

FFFFFFFF with flipper

FFFFFFFF

00000000

00000000 with even parity

55555555

AAAAAAAA

33333333

00122

CCCCCCCC

0F0F0F0F

F0F0F0F0

00FF00FF

FF00FF00

11111111

22222222

44444444

66666666

77777777

88888888

99999999

BBBBBBBB

DDDDDDDD

EEEEEEEE

4.31 The normal X-ray program trace setup (Figure 4) should be used for the CRBTST program. If a more detailed analysis of a particular problem is required, command or memory traces can be used. Both the phase selection and control parameters are contained in the test select table. A typical parameter setup and execution for the CRBTST program is shown in Figure 16.

4.32 If the program encounters an error during execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 17 are valid.

Command-Response Bus Matcher Test (MTCTST)

4.33 The MTCTST (version B02) program verifies the basic operation of the bus matcher circuits. The program is comprised of six test phases; the names and functions of these phases are listed in Table 4.

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4.34 The normal X-ray program trace setup (Figure 4) should normally be used for the MTCTST program. If desired, however, a CMD (command bus) trace may be set up to compare the actual bus data to the matchers for fault analysis.

4.35 The only parameter required for the MTCTST program is the selection of the BIU copy. Operational parameters are for PCDC display and routine mode. (Refer to Figure 18a.) For a typical phase selection, refer to Figure 18b.

4.36 Normal X-ray program execution is used for this program. However, for phases 2 and 3, which require a backplane strap (fault insertion), there are special instructions for execution. If X-PARM ADDR 2 is marked for PCDC display (default), at the beginning of phases 2 and 3 the PCDC display informs the operator to STRAP TX - PIN 52 to 53 ON T09 for phase 2 and A27 for phase 3. The program waits for the operator to complete the strapping and perform the following:

(a) Depress the ENTRY START pushbutton.

(b) Enter C via the keypad.

(c) Depress the FUNCTIONS DATA FCN pushbutton.

4.37 Upon completion of the test, the program prompts the operator (via the PCDC display) to REMOVE STRAP and waits for the operator's PCDC entry. A bad entry results in a display of BAD ENTRY.

4.38 A typical MTCTST execution is shown in Figure 18c. If the program encounters an error during execution, the error displays shown in Figure 19 are valid.

Processor Control and Display Console Test (CDITST)

4.39 The CDITST (version B01) program verifies the basic operation and interface of the PCDC and of the Control and Display Interface (CDI). Since the PCDC is a manual device, this test program is structured for man-machine interface operations. The operator must enter via the keypad predetermined patterns and

verify the resulting displays. The program provides the necessary internal hardware instructions for reception and sending, and verifies the internal hardware functions associated with each test. The program reports test success or failure via the system monitor X-ray program trace mechanism.

4.40 The tests performed by the CDITST program are as follows:

(a) Initial PCDC display.

(b) ASCII character input and echo.

(c) Alphabetic character display.

(d) Decimal numberic character display.

(e) Initialization pushbutton code test.

(f) Message Class Suppression (MCS) pushbutton code test.

(g) Data function pushbutton code test.

(h) Variable input formatted echo character test.

(i) Software counter display.

4.41 The normal X-ray program trace setup (Figure 4) is used for the CDITST program. There are no phase select or parameter control input requirements for this program. A typical CDITST execution is shown in Figure 20. If an X-ray program trace dump occurs during the execution of the manual input procedure (Figure 20), the error displays shown in Figure 21 are valid.

Memory Interface Unit Test (MIUTST)

4.42 The MIUTST (version B01) program tests basic MIU operations. The program of comprised of six test phases; the names and functions of these phases are listed in Table 5.

4.43 The normal X-ray program trace setup (Figure 4) is generally used for the MIUTST program. However, it may be necessary to set up a command bus trace for more extensive fault analysis. Typical sequence control, parameter control,

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and execution for the MIUTST program are shown in Figure 22. If the program encounters an error during execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 23 are valid.

Basic Memory Test (MUTEST)

4.44 The MUTEST (version B26) program tests basic memory operations. The program is comprised of seven test phases; the functions of these phases are listed in Table 6. All memory operations are unmapped and use the BDOR address format. The MUTEST program contains parameter controls that allow for a PCDC display of the current memory unit under test. It also contains a routine control that allows the specified memory unit to be routined with run and error counts for prolonged periods of time.

4.45 The normal X-ray program trace setup (Figure 4) is generally used for the MUTEST program. However, for specific fault isolation it may be necessary to use other types of traces, such as command or memory traces. Typical phase select control, parameter control, and execution for the MUTEST program are shown in Figure 24. If the routine parameter is set for program execution (Figure 24c), start the program with normal execution. Then, at periodic intervals, restart the trace setup to capture the updated total RUN and ERROR counts in REG4.

4.46 If the program detects a fault during normal execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 25 are valid.

Bus Interface Unit Test (BIUTST)

4.47 The BIUTST (version B25) program verifies the basic operation of the BIU by testing the PC MAP, and by extensively exercising the enable/disable read status on all bus configurations. There are no control parameters that must be input for this program.

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4.48 The peripheral controller MAP tests are performed with an initial configuration of SCB0, SRB0, BIU0, BUS PTR 0, RESET DWRT, and DSRB BIU0,1. The PC MAP tests are as follows:

(a) Address test. Each peripheral controller MAP address is accessed and written with data. Each address is then read back and the data checked.

(b) Write disable test. The BIU is set for DWRT (disable write), and an attempt is made to overwrite the peripheral controller MAP data with all F's. The peripheral controller MAP is then read back to ensure that the data was disabled from being overwritten.

(c) Pattern test. Each bit position for each individual peripheral controller MAP address is written and then read back for verification.

These tests are repeated for BIU0 and SCB1, and for BIU1 and SCB0 and 1.

4.49 The SRB status tests shown in Figure 26 verify the enable/disable at the read status for each BIU copy, for all configurations of the command and response buses.

4.50 The normal X-ray program trace setup (Figure 4) is generally used for the BIUTST program. However, for more specific problem resolution, it may be necessary to use a different type of trace setup, such as a command trace. The normal X-ray program execution is used for the BIUTST program. Typical BIUTST phase select and execution is shown in Figure 27.

4.51 If the program encounters an error during normal execution (FR-ADDR = 5, TO-ADDR = 5), the error displays shown in Figure 28 are valid.

Peripheral Access Unit Test (PAUTST)

4.52 The PAUTST (version B21) program tests the basic operation of the Peripheral Access Unit (PAU), Peripheral Controller (PC), Peripheral Unit Matrix (PUM), and the associated interfaces. The PAUTST program is comprised of five phases; the functions of these phases are listed in Table 7. The

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phase functions are performed for either or both BIU's on either or both buses, depending upon the parameter control selection.

4.53 The normal X-ray program trace setup (Figure 4) and execution mode are generally used for the PAUTST program. If more detailed problem analysis is desired, CMD and PC traces can be used. The error display for phases 4 and 9 are not adequately defined for a specific fault associated with a specific function. Therefore, it will probably be necessary to modify the trace stop address to the subroutine error display (for version B26). This is location 313 with a regressive trace. The operator must then reference the listing for subroutine APU (52) to find the function being performed as associated with the error.

4.54 Typical PAUTST phase select, parameter control, and execution are shown in Figure 29. If an error is encountered during normal program execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 30 are valid.

Magnetic Tape Unit Test (MTUTST)

4.55 The MTUTST (version B04) program verifies the basic operation of the system Magnetic Tape Unit (MTU) and the associated interfaces. The MTUTST program is comprised of five phases, the names and functions of which are listed in Table 8. Phase 0 includes four tests, while the remaining phases consist of one test each. The phases for the MTUTST program must be executed in a specific sequence (paragraph 4.56).

4.56 The normal X-ray program trace setup (Figure 4) is generally used for the MTUTST program. If more detailed problem analysis is required, CMD or PC traces may be used. The normal X-ray program execution is used for the MTUTST program. However, the program phases must be executed in the following sequence (phase 0 is always run):

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(a) Phases 0 through 3 (default).

(b) Phases 0 and 4 only.

(c) Phases 0 and 3 only.

4.57 Typical MTUTST parameter control selection, phase selection, and execution are shown in Figure 31. If the program detects a fault during normal execution (FR-ADDR = 6, TO-ADDR 5), the error displays shown in Figure 32 are valid.

General Register and Next Execute Program Counter Test (GRNEPCTST)

4.58 The GRNEPCTST (version B33) program verifies proper operation of General Registers (GR's) 0 through 7 as used by system software (micro A-file registers 0 through 7), and proper operation of the micro-software Next Execute Program Counter (NEPC).

4.59 General Register Test. For this test, the A-file registers 0 through 7 are verified by performing a checkboard test of the following patterns, in the sequence shown:

FFFFFFFF

00000000

55555555

AAAAAAAA

33333333

CCCCCCCC

0F0F0F0F

F0F0F0F0

00FF00FF

FF00FF00

11111111

77777777

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4.60 NEPC Test. The NEPC is verified by initializing memory (and associated memory map) with selected system (macro) instructions and verifying the micro-decode NEPC of the executed macro-instructions. The sequence of operation is as follows:

(a) Zero memory locations 0 through 8FFF.

(b) Memory initialized with macro-instructions for Process Store (PS) pages 0, 1, 2, and 4, with the last PS location being a HELP instruction.

(c) The memory map is initialized and the macro-instruction is fetched and decoded.

(d) The macro-instructions executed are listed in Table 9.

4.61 The normal X-ray program trace setup (Figure 4) is used for the GRNEPCTST program. There are no selectable parameters associated with the program. Typical GRNEPCTST phase select and execution are shown in Figure 33. If an error is detected during normal program execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 34 are valid. (There are no error displays specifically associated with the general register test, nor are there phase numbers assigned to that test.)

Stack Test (STKTST)

4.62 The STKTST (version B02) program verifies proper operation of the system's instruction stack and associated register and counter. The program is comprised of nine phases; the functions of these phases are listed in Table 10. All phase functions are verified through the use of FETCH instructions and the DECODE PLA.

4.63 The normal X-ray program trace setup (Figure 4) is used for the STKTST program. Typical phase selection, parameter control, and execution for this program are shown in Figure 35. If an error is detected during normal program execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 36 are valid.

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Decode PLA Test (DCDTST)

4.64 The DCDTST (version B26) program verifies the proper operation of all data paths used by a macro-instruction (system software) coming from memory and going through a decode operation to a micro-location. The functions verified are as follows:

(a) RECEIVER MUX

(b) INSTRUCTION LATCH

(c) INSTRUCTION STACK

(d) I-REGISTER LEFT

(e) I-REGISTER RIGHT

(f) DECODE PLA

4.65 The DCDTST program is comprised of three phases; the functions of these phases are listed in Table 11. The firmware FLAG must be operational for the performance of the DCDTST test program.

4.66 The normal X-ray program trace setup (Figure 4) is used for the DCDTST program. There is no phase selection associated with this program, but there are operator input functions that control the reporting of errors detected. Typical DCDTST error reporting parameter selection, parameter control, and execution are shown in Figure 37.

4.67 If the program detects an error during normal execution (FR-ADDR = 6, TO-ADDR = 5), the error displays shown in Figure 38 are valid.

Table 1. Program Execution Sequence.

SEQUENCE NUMBER	PROGRAM NAME	FUNCTIONS TESTED
1	SEQTST	Basic central processor unit operation
2	ALUTST	Main central processor unit data structure
3	CLKTST	Master and standby clock control
4	TTEST	Operation of the multiple test selection field
5	BUSCTL	Bus timer logic
6	BUSTEST	Basic bus configuration; memory map; SPR, refresh, and PAU timers; utility counter; IPL ROMS; bus history stack
7	CRBTST	Command and response buses
8	MTCTST	Left/right and A/B matchers
9	CDITST	PCDC - control and display interface
10	MIUTST	Memory interface units
11	MUTEST	Basic memory units
12	BIUTST	Bus interface unit and peripheral controller map
13	PAUTST	Peripheral access unit and peripheral control unit
14	MTUTST	Magnetic tape unit and associated logic/ interfaces
15	GRNEPCTST	General registers and next execute program counter
16	STKTST	Instruction stack, instruction address register, next fetch counter, IREG, VFLAG, BMG
17	DCDTST	RCVR MUX, instruction latch/stack, IREG, DECODE PLA

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Table 2. ALUTST Test Program Phases.

PHASE	FUNCTION
0	Basic skip checks
1	"A" latch test
2	Basic file checks
3	Basic counter check
4	Counter addressing of B-file checks
5	BMG (CNTR) B-operand checks
6	Basic ALU checks
7	Carry and overflow checks
8	Literal checks
9	BLU bit test checks
A	SPR checks
B	Special-case operands-to-file checks
C	Basic shift-register checks
D	Remaining shift-register checks
E	Data structure to system monitor interface

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Table 3. BUSTST Test Program Tests and Phases.

TEST	PHASE	FUNCTION
0	1 through 4	MAP test - map address write/read
	5 and 6	MAP test - map pattern write/read
1		SPR timer test
2		Counter test
3		Refresh timer test
4		PAU timer test
5	1	Bus/control test - bus configuration
	2	Bus/control test - parity error generation
	3	Bus/control test - ripple test
	4	Bus/control test - parity/flipper bit
	5	Bus/control test - data pattern
6		IPL ROM - left half
7		IPL ROM - right half
8	1	Bus history stack test - stack pointer
	2	Bus history stack test - stack freeze
	3	Bus history stack test - bus history function

00134

Table 4. MTCTST Test Program Phases.

PHASE	TEST NAME	FUNCTION
0	L MATCH TX	Verifies command matcher left using command buses 0 and 1, and response buses 0 and 1 by detecting a matcher error for writing data even parity.
1	R MATCH TX	Verifies command matcher right using the same process that is used for L MATCH TX.
2	L MATCH	Requires that a backplane strap be installed connecting SCB 1R TX to SCB 0R TX. Verifies that NOTX inhibits bus command and also performs parity bit, flipper bit, and ripple data tests for left command matcher errors.
3	R MATCH	Requires a backplane strap connecting SCB 1L TX to SCB 0L TX. Performs the same tests as L MATCH for right command matcher.
4	A MATCH	Verifies response A matcher by performing write data even parity, parity and flipper bits, and ripple data tests.
5	B MATCH	Verifies response B matcher by performing the same type of test as A MATCH.

00135

Table 5. MIUTST Test Program Phases.

PHASE	TEST NAME	FUNCTION
0	DISABLE PHASE	All equipped MIU's are disabled and each MIU is checked to ensure that it does not respond to its individual address.
1	ADDRESS RECOGNITION PHASE	Ensures that all equipped MIU's respond only to their own individual addresses.
2	READ RESPONSE ALGORITHM PHASE	Ensures that all equipped MIU's respond to specified read commands.
3	ENABLE/DISABLE STATUS PHASE	Ensures that all equipped MIU's can enable and disable read and write operations via their individual status bits.
4	NONFUNCTIONAL STATUS PHASE	Ensures that a write status command with bits 0 through 5 set to logic 1's does not cause a status change.
5	ACROSS BUS STATUS PHASE	Ensures that one side of an MIU can be write enabled, read disabled, write disabled, status read and not read from the other side.

00136

Table 6. MUTEST Test Program Phases.

PHASE	FUNCTION
0	An attempt is made to initialize the MIU's and to reset all error conditions.
1	Data with even parity is written into the first location of the specified memory unit. A check is made to ensure that a parity error occurs on a read of that location.
2	All logic 0's are written into the specified memory unit and then verified by reading each location.
3	All logic 1's are written into the specified memory unit and then verified.
4	Each individual address is written into the associated location and then verified.
5	A single set bit is shifted across all 32 bit positions (numbered 31 through 0) and verified for all specified memory units.
6	Verifies the operation of the flipper bit by setting both logic 1's and 0's and checking for the inversion of the data.

00137

Table 7. PAUTST Test Program Phases.

PHASE	FUNCTION
0	Initialize CP's, buses, BIU, and PAU
1	Verify PC STATUS READ/WRITE operation
2	Verify PC DATA REGISTER operation
3	Verify PU DATA REGISTER operation
4	Verify BIU disable write operation

00138

Table 8. MTUTST Test Program Phases.

PHASE	NAME	TEST	FUNCTION
0		0	BIU and PCU initialization for SCB0,1; SRB0; BIU0,1; and selected PCU and copy (default = PCU0,0)
		1	PCU: write control mode; MOD4 = 0; reset TBF, RDF, SDF, FCF; set UAF
		2	PCR: address echo check
		3	PCR; data echo check
1	MASTER CLEAR TEST		MTU should be on-line, loaded with a magnetic tape with write ring installed; verifies IR, BOT, ONL, and TRDY = 1
2	FIFO TEST		Write A's and 5's into First-In-First-Out (FIFO) word 0; verifies A's and 5's on reading FIFO
3	READ ONLY TAPE TEST		Reads magnetic tape test pattern; verifies ripple bit patterns
4	READ ONLY TAPE GENERATION		Writes specific test patterns on magnetic tape; verifies proper MTU logic operation

00139

Table 9. Macro-Instructions Executed in NEPC Test.

MICRO-LOCATION VECTOR	INSTRUCTION	DECODE
"100"	TRAP 00	MAP ERROR
"102"	TRAP 02 (HELP)	END TEST
"108"	CPH CHOX	COPY RH.H+Z TO RX LEFT
"10C"	CPH CHXO	LOAD OVERFLOW, Y%=SAR
"118"	TPR XO	UNCOND XFR W/O LINK
"168"	CPH HOGH	COPY RY.H+Z TO RX RIGHT
"16C"	CPH HXOGY	COPY RY.H+Z TO SAR

Table 10. STKTST Test Program Phases.

PHASE	FUNCTION
0	Initialize memory to 0
1	Verify instruction latch/stack data patterns; 0-0, F-F, 5-5, A-A, 3-3, C-C, 0F-0F, F0-F0, 00FF-00FF, and FF00-FF00
2	Verify instruction latch/stack addressing
3	Verify Instruction Address Register (IAR) operation
4	Verify Next Fetch Program Counter (NFPC) operation
5	Verify self-interrupt counter operation
6	Verify Instruction Register (IREG) operation
7	Verify the operation of the VFLAG and the following errors: copy 00, DATA LOST, and DATA TO
8	Verify Bit Mask Generator (BMG) operation

Table 11. DCDTST Test Program Phases.

PHASE	FUNCTION
0	CMC initialization
1	MIUO, copy 0, MUO is loaded with all unique macro instructions possible after being initialized to all 0's
2	Each macro instruction is pipeline fetched, decoded, and checked for correct decode vector

00142

ROMSIM LOC (HEX)	FUNCTION
5	COMMON LOCATION FOR BOTH SUCCESSFUL (FROM LOC 7) AND ERROR (FROM LOC 6) TEST RESULTS - INTERNAL CONTROL
6	INDICATES A TEST ERROR OCCURRED (TO LOC 5) - INTERNAL CONTROL
7	INDICATES A SUCCESSFUL TEST OCCURRED (TO LOC 5) - INTERNAL CONTROL
8	SEQUENCE CONTROL TABLE - PHASE SELECTION - USER CONTROL (X-SEQUENCE ADDR=0) 0 1 15 PHASE 1 PHASE 2 BIT RESET = SKIP PHASE BIT SET = RUN PHASE PHASE 16 DEFAULT VALUE = "FFFF" = RUN ALL PHASES
9	SEQUENCE CONTROL TABLE - LOOP CONTROL - USER CONTROL (X-SEQUENCE ADDR=1) 0 1 15 PHASE 1 PHASE 2 BIT SET = LOOP ON PHASE BIT RESET = DO NOT LOOP ON PHASE PHASE 16 DEFAULT VALUE = "0000" = DO NOT LOOP ON ANY PHASE
300	PARAMETER CONTROL TABLE - LENGTH OF TABLE - INTERNAL CONTROL - THE LENGTH OF THE TABLE IS X-RAY DEPENDENT
301 . . . 3FF	PARAMETER CONTROL TABLE - ENTRIES - USER CONTROL (X-PARM ADDR=0 THRU FE) THE ENTRIES IN THE TABLE ARE VARIABLE (OPEN ENDED) AND THEIR DEFINITIONS ARE X-RAY DEPENDENT

Figure 1. User-Oriented X-Ray Program Locations.

00143

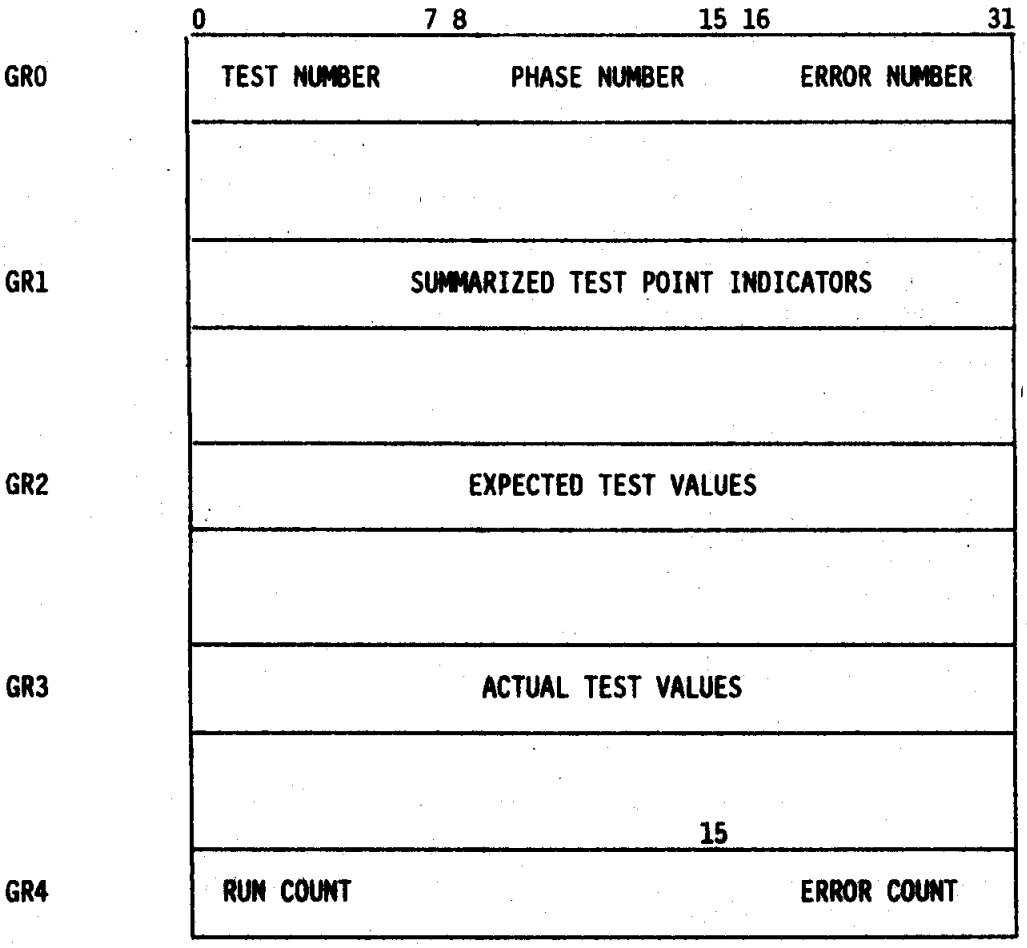


Figure 2. Standard Microdiagnostic Register Formats.

00144

0	4	8	12	16	20	24	28																								
CP0	CP1	CP2	CP0	CP1	CP2	MEM	INTR	INTR	PARITY	NOTA	NOTX	DATA	L MATCHER	R MATCHER	A MATCHER	B MATCHER	DMA TERM	ANY REQ	ANY ERR	CDI RDY	DATA LOST	SPR TO	COPY OO	PTC REQ	SLF INT	PAU TO	DMA RDY	CDI REQ			
CP0 VO	CP1 VO	CP2 VO	CP0 MSTR	CP1 MSTR	CP2 MSTR	CP0 ERR	CP1 ERR	CP2 ERR	MEM RTN	INTR 1	INTR 2	PARITY	NOTA	NOTX	DATA TO	L MATCHER	R MATCHER	A MATCHER	B MATCHER	DMA TERM	ANY REQ	ANY ERR	CDI RDY	DATA LOST	SPR TO	COPY OO	PTC REQ	SLF INT	PAU TO	DMA RDY	CDI REQ

CP0 VO = CENTRAL PROCESSOR 0 VOTED OUT
CP1 VO = CENTRAL PROCESSOR 1 VOTED OUT
CP2 VO = CENTRAL PROCESSOR 2 VOTED OUT
CP0 MSTR = CENTRAL PROCESSOR 0 MASTER
CP1 MSTR = CENTRAL PROCESSOR 1 MASTER
CP2 MSTR = CENTRAL PROCESSOR 2 MASTER
CP0 ERR = CENTRAL PROCESSOR 0 ERROR
CP1 ERR = CENTRAL PROCESSOR 1 ERROR
CP2 ERR = CENTRAL PROCESSOR 2 ERROR
MEM RTN = MEMORY RETURN SCHEDULED
INTR 1 = INTERRUPT LEVEL 1
INTR 2 = INTERRUPT LEVEL 2
PARITY = RECEIVED DATA PARITY ERROR
NOTA = NO BUS COMMAND ACKNOWLEDGE
NOTX = NO BUS RETURN DATA STROBE
DATA TO = DATA TIME OUT (3.2 µs)
L MATCHER = LEFT COMMAND BUS MATCH ERROR
R MATCHER = RIGHT COMMAND BUS MATCH ERROR
A MATCHER = SUB BUS A RESPONSE MATCH ERROR
B MATCHER = SUB BUS B RESPONSE MATCH ERROR
DMA TERM = DIRECT MEMORY ACCESS TERMINATION
ANY REQ = ANY REQUEST
ANY ERR = ANY ERROR
CDI RDY = CONTROL DISPLAY INTERFACE READY
DATA LOST = RESPONSE DATA NOT PICKED UP BY CP
SPR TO = SOFTWARE TIME OUT (2 µs COUNTER)
COPY OO = WRITE VIOLATION OR NONEXISTENT MEMORY
PTC REQ = PROGRAMMER TEST CONSOLE REQUEST BY FIRMWARE
SLF INT = SELF INTERRUPT BY FIRMWARE
PAU TO = PERIPHERAL ACCESS UNIT TIME OUT (2.6 µs)
DMA RDY = DIRECT MEMORY ACCESS READY
CDI REQ = CONTROL DISPLAY INTERFACE REQUEST FROM PCDC

Figure 3. General Register 2 Data Contents.

00145

```
I*<TRACE>

**TRACE**
1 COPY (D,1,B) = <B>
2 MODE (P,R) = <R>
3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = <INS>
4 START (ADDR,EXT,IMMED) = <IMMED>
5 STOP (ADDR,EXT,OVFL) = <ADDR>
STOP ADDR = <5>
EVENTS = <10>
READY (Y,N,E,X,A) = <X>

**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = <L>

**CARTRIDGE IN OK -- REWINDING**

**VERIFY STARTED**

**VERIFY COMPLETED**
```

Figure 4. Typical Trace Setup.

00146

```
**TRACE**
1 COPY (O,1,B) = B
2 MODE (P,R) = R
3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = INS
4 START (ADDR,EXT,IMMED) = IMMED
5 STOP (ADDR,EXT,OVFL) = ADDR
STOP ADDR = 5
EVENTS = 10
READY (Y,N,E,X,A) = Y

**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = L

**CARTRIDGE IN OK -- REWINDING**

1SEQTST.B01 5-27-78 VERSION 1.1

**VERIFY STARTED**

**VERIFY COMPLETE**
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
00000000 11111111 22222222 33333333 44444444 55555555 66666666 77777777

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  0022    00007   00005   0   00000000
0002          000DD   00007   0   00000000
0003          000DB   000DC   7   77777777
0004          000DA   000DB   6   66666666
0005          000D9   000DA   5   55555555
0006          00008   000D9   4   44444444
0007          000D7   00008   3   33333333
0008          000D6   000D7   2   22222222
0009          000D5   000D6   1   11111111
000A          000D2   000D5   0   00000000
000B          00045   00042   7R      7777
000C          00047   00045   7L  7777
000D          002AB   00040   7   00000000
000E          001AA   002AA   6R      6666
000F          003AA   001AA   6L  6666
0010          001AD   003AA   5R      5555

  REG0     REG1     REG2     REG3     REG4     REG5     REG6     REG7
00000000 11111111 22222222 33333333 44444444 55555555 66666666 77777777

**MONITOR** V1.2
```

Figure 5. Typical SEQTST Trace Setup and Execution.

00147

REG0 ERROR NUMBER	FAILING FUNCTION
00000002	Unconditional skip insturction
00000003	Skip false instruction
00000004	Skip true instruction
00000005	Skip true not instruction
00000006	Execute (and return) instruction
00000007	Execute (and return) instruction
00000008	Execute (and return) instruction
00000009	Execute (and return) instruction
0000000A	Call (and return) instruction
0000000B	Call (and return) instruction
0000000C	Call (and return) instruction
0000000D	Call (and return) instruction
0000000E	Call (and return) instruction
0000000F	Call (and return) instruction
000000010	Call (and return) instruction
000000010	Call (and return) instrcution

The trace dump should display the general registers as:

REG0	REG1	REG2	REG3	REG4	REG5	REG6	REG7
0--0	1--1	2--2	3--3	4--4	5--5	6--6	7--7

Figure 6. Valid Error Displays for Failure of Normal Trace Setup.

00148

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0

0000  0020 -

X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  FFFFFFFF  55555555  AAAAAAAA  33333333  CCCCCCCC  0F0F0F0F  F0F0F0F0

LINE  EVENTS  FR-ADDR  TO-ADR  GR  GR-DATA

0001  0082    00007    00005   0   00000000
0002          0002F    00007   0   00000000
0003          001CE    001CF   0   00000000
0004          001CD    001CE   1   FFFFFFFF
0005          001CB    001CC   2   55555555
0006          001C9    001CA   3   AAAAAAAA
0007          001C7    001C8   4   33333333
0008          001C5    001C6   5   CCCCCCCC
0009          001C3    001C4   6   0F0F0F0F
000A          001C1    001C2   7   F0F0F0F0
000B          002C1    002C2   7R      FFFF
000C          002C0    002C1   7R      BAFF
000D          002BF    002C0   7R      FF00
000E          002BE    002BF   7R      BB00
000F          002B8    002B9   7R      00FF
0010          002B7    002B8   7R      00BB

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  FFFFFFFF  55555555  AAAAAAAA  33333333  CCCCCCCC  0F0F0F0F  F0F0F0F0

**MONITOR** V1.2
```

Figure 7. Normal Execution Mode for ALUTST Test Program.

00149

REG0 PHASE	ERROR NUMBER	FAILING FUNCTION
0000	0FFD	CLOCK ERROR
0000	0FFE	SYNC ERROR
0000	0001	ALU NOT ZERO SKIP
0000	0002	ALU ZERO SKIP
0000	0003	ALU ZERO NOT SKIP
0000	0004	ALU NOT ZERO NOT SKIP
0001	0000	A FILE LATCH (LEFT) ALL ZERO'S
0001	000F	A FILE LATCH (LEFT) BIT 15
0001	000E	A FILE LATCH (LEFT) BIT 14
0001	000D	A FILE LATCH (LEFT) BIT 13
0001	000C	A FILE LATCH (LEFT) BIT 12
0001	000B	A FILE LATCH (LEFT) BIT 11
0001	000A	A FILE LATCH (LEFT) BIT 10
0001	0009	A FILE LATCH (LEFT) BIT 9
0001	0008	A FILE LATCH (LEFT) BIT 8
0001	0007	A FILE LATCH (LEFT) BIT 7
0001	0006	A FILE LATCH (LEFT) BIT 6
0001	0005	A FILE LATCH (LEFT) BIT 5
0001	0004	A FILE LATCH (LEFT) BIT 4
0001	0003	A FILE LATCH (LEFT) BIT 3
0001	0002	A FILE LATCH (LEFT) BIT 2
0001	0001	A FILE LATCH (LEFT) BIT 1
0001	0000	A FILE LATCH (LEFT) BIT 0
0002	0222	A AND B FILE DATA MANIPULATION CHECKSUM = "FFE0"
0003	0333	COUNTER OPERATION FINAL RESULT = "0002"
0004	0444	B FILE ADDRESSING FROM COUNTER = CHECKSUM = "FF01"
0005	0555	BMG (CNTR) B-OPERAND - CHECKSUM = "FFF0"
0006	0666	BASIC ALU OPERATION - FINAL RESULT = "0001"
0007	0777	CARRY AND OVERFLOW - FINAL RESULT = "00FF"
0008	0888	LITERALS - FINAL RESULT = "01FA"
0009	0999	ALU BIT TEST - FINAL RESULT = "0000"
000A	0AAA	SPR CHECK - FINAL RESULT = "199A"
000B	0BBB	SPECIAL CASE OPERANDS - FINAL RESULT = "CCCD"
000C	0CCC	SHIFT REGISTER - FINAL RESULT = "E668"
000D	0DDD	SHIFT CHECKS - FINAL RESULT = "3FCE"
000E	REQUIRES VISUAL	CHECK BY OPERATOR FOR THE FOLLOWING:
	REG0 = 00000000	
	REG1 = FFFFFFFF	
	REG2 = 55555555	
	REG3 = AAAAAAAA	
	REG4 = 33333333	
	REG5 = CCCCCCCC	
	REG6 = 0F0F0F0F	
	REG7 = F0F0F0F0	

Figure 8. Valid Error Displays for Failure and Normal Trace Setup for ALUTST.

00150

```
I* TRACE

**TRACE**
1 COPY (0,1,B) = B
2 MODE (P,R) = R
3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD) = INS
4 START (ADDR,EXT,IMMED) = IMMED
5 STOP (ADDR,EXT,OVFL) = ADDR
STOP ADDR = 5
EVENTS = 10
READY (Y,N,E,X,A) = X

**X-RAY**
X-RAY (S,L,E,EM,K,T,P,C) = L

**CARTRIDGE IN OK --REWINDING**

1CLKTST.B01 5-27-78 VERSION 1.1

**VERIFY STARTED**

**VERIFY COMPLETE**
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000006  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR   GR  GR-DATA

0001  000A    00007   00005    0   00000006
0002          0001E   00006    0L  0000
0003          0001D   0001E    0R      0006
0004          00000   00000    0R      0000
0005          00000   00000    0R      0000
0006          00413   00000    0R      0000
0007          00401   0040A    0L  0001
0008          003FF   00400    0R      0000
0009          00282   00282    0R      0000
000A          00000   00000    0R      0000

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00010000  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

**MONITOR** V1.2
```

Figure 9. Typical CLKTST Trace Setup and Execution.

REGO PHASE	REGO ERROR NUMBER	FAILING FUNCTION
0001	0002	CLOCK ERRORS DID NOT RESET
0001	0003	ACTIVE CLOCK DID NOT SWITCH OVER
0001	0004	CLOCK ERROR NOT SET
0001	0005	CLOCK SYNC ERROR NOT SET
0001	0006	CLOCK "A" DID NOT SWITCH TO CLOCK "B"
0001	0007	CLOCK ERROR OR CLOCK SYNC ERROR NOT RESET
0002	0008	CLOCK ERROR MALFUNCTION
0002	0009	CLOCK "B" ACTIVE
XXXX	0001	NO CLOCK ERRORS ON INTERRUPT

NOTE: XXXX = DON'T CARE OR ANY PHASE.

Figure 10. Valid Error Displays for Failure of Normal Trace Setup for CLKTST.

00152

REG 0R: OFFD = CLOCK ERROR; OFFE = SYNC ERROR

REG 0L:
- 1XX0 = CP0 V0
- X1X0 = CP1 V0
- XX10 = CP2 V0

REG 1L:
- 1XX0 = CP0 MSTR
- X1X0 = CP1 MSTR
- XX10 = CP2 MSTR

REG 2L:
- 1XXX = CP0 ERR
- X1XX = CP1 ERR
- XX1X = CP2 ERR
- XXX1 = NON MEM

REG 3L:
- 1XXX = INTR1
- X1XX = INTR2
- XX1X = HBAR
- XXX1 = YNEZ

REG 4L:
- 1XX0 = PARITY
- X1X0 = NOTA
- XX10 = NOTX

REG 5L:
- 1XXX = L MATCH
- X1XX = R MATCH
- XX1X = A MATCH
- XXX1 = B MATCH

REG 6L:
- 1XXX = D MATERM
- X1XX = B CLOCK
- XX1X = CLK ERROR
- XXX1 = CSYNCERR

REG 7L:
- 1XXX = DATA TO
- X1XX = DATA LOST
- XX1X = SPR TO
- XXX1 = COPY 00

Figure 11. Register Display for TTEST.

00153

```
REG 7R:

     0001 = INTR1 DID NOT RESET ON R_ERR

     0010 = INTR2 DID NOT RESET ON R_ERR

     0040 = INTR2 DID NOT SET   ON S_ERRH

     0004 = INTR1 DID NOT SET   ON S_ERRH
```

Figure 12. Valid Error Displays for Failure of Normal Trace Setup for TTEST.

MASTER CP	SUB-BUS	COMMAND BUS	RESPONSE BUS	BIU	COPY
0	0A,1A	0/1	0/1	0/1	0/1
1	0A,1B	0/1	0/1	0/1	0/1
2	0B,1A	0/1	0/1	0/1	0/1

Figure 13. Bus Configurations.

00155

BIT	DEFINITION
0-2	DON'T CARE
3	SYSTEM RESPONSE BUS; 0=BUS0, 1=BUS1
4-8	DON'T CARE
9	SYSTEM COMMAND BUS; 0=NO, 1=BUS1
10	CP SUBBUS PBT 1L; 0=A, 1=B
11	CP SUBBUS PBT 1R; 0=A, 1=B
12	CP SUBBUS PBT 0L; 0=A, 1=B
13	CP SUBBUS PBT 0R; 0=A, 1=B
14	BIU COPY; 0=COPY0, 1=COPY1
15	SYSTEM COMMAND BUS; 0=NO, 1=BUS0

(Program default parameter is 0000)

```
I* X-RAY
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0
0000 0000 - (Operator Input Selection)
            / = No change - use default
```

Figure 14a. Bus Configuration Parameters.

```
I* X-RAY
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR=1 IPL LEFT ROM CRC
0001 CE4C - DEFAULT = VERSION 1 PROMS
X-PARAM ADDR=2 IPL RIGHT ROM CRC
0002 B1D0 - DEFAULT = VERSION 1 PROMS
```

Figure 14b. IPL Parameters.

Figure 14. Bus Configuration and IPL Parameters.

```
I* X-RAY
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - (Default set to run all tests)
          -  8000 = MEMORY MAP TEST ONLY
          -  4000 = SPR TIMER TEST ONLY
          -  2000 = COUNTER TEST ONLY
          -  1000 = REFRESH TIMER TEST ONLY
          -  0800 = PAU TIMER TEST ONLY
          -  0400 = BUS CONF TEST ONLY
          -  0200 = IPL L ROM TEST ONLY
          -  0100 = IPL R ROM TEST ONLY
          -  0080 = BUS HISTORY TEST ONLY
```

Figure 15a. Test Selection.

```
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

     04   0009      FLIPPER DATA - FLIPPER BIT NOT SET
     04   000A      FLIPPER DATA - DATA FLIPPED INCORRECTLY
     05             PATTERN TEST -
      ALL OF THE ABOVE ERRORS ALSO APPLY FOR THIS TEST

06   00   0001      IPL LEFT ROM - CRC CHECKSUM DID NOT MATCH EXPECTED VALUE
07   00   0001      IPL RIGHT ROM - CRC CHECKSUM DID NOT MATCH EXPECTED VALUE
08   00   0001      BUS HISTORY - POINTER NOT LOADING PROPERLY
08   01   0002      BUS HISTORY - POINTER NOT DECREMENTING PROPERLY
08   02   0003      BUS HISTORY - POINTER WILL NOT FREEZE
08   03   0004      BUS HISTORY - BUS HISTORY DATA MISMATCH
08   03   0005      BUS HISTORY - SPILL PS AND PAGE INFO INCORRECT
```

Figure 15b. Execution.

Figure 15. Typical BUSTST Test Selection and Execution.

00157

```
X-RAY (S,L,E,EM,K,T,P,C) = C
X-SEQNCE ADDR = 0
0000 8000 - Default set for Response Bus 0, PCDC Display.
          - 4000 = Response Bus 1
          - 2000 = Ripple Test
          - 1000 = Checker Test
          - XXX1 = No PCDC Display
          - F000 = Normal Selection

EXECUTION

X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00FF0000  XXXXXXXX  EEEEEEEE  EEEEEEEE  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  0068    00007   00005   0   00FF0000
0002          0004A   00007   0   00FF0000
0003          00099   0009A   2R      EEEE
0004          00098   00099   2L  EEEE
0005          0008D   0008D   3   EEEEEEEE
0006          00070   00071   2   EEEEEEEE
0007          00099   0009A   2R      DDDD
0008          00098   00099   2L  DDDD
0009          0008D   0008D   3   DDDDDDDD
000A          00070   00071   2   DDDDDDDD
000B          00099   0009A   2R      BBBB
000C          00098   00099   2L  BBBB
000D          0008D   0008D   3   BBBBBBBB
000E          00070   00071   2   BBBBBBBB
000F          00099   0009A   2R      9999
0010          00098   00099   2L  9999

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00FF0000  XXXXXXXX  99999999  BBBBBBBB  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX
```

Figure 16. Typical CRBTST Parameter Setup and Execution.

00158

REG0 = PHASE AND ERROR NUMBER
REG1 = INTERNAL TEST POINTS
REG2 = EXPECTED DATA
REG3 = ACTUAL DATA
REG4 = LAST BUS DATA SENT
REG5 = LAST BUS COMMAND SENT
REG6 = LAST BUS DATA RECEIVED
REG7 = DATA RECEIVED AFTER MASKING

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
0000	00D0	CLOCK ERROR
0000	00E0	SYNC ERROR
0000	00FF	NO TEST SELECTED
0000	0008	NO CP SELECTED MASTER
0000	0007	NO RESPONSE FROM CDI
0000	0006	NOTA ON MIU STATUS WRITE
0000	0005	EXPECTED AND ACTUAL DATA READ MISMATCH
0000	0004	PARITY, NOTA, NOTX, DATA TO, OR DATA LOST ON MIU READ
0000	0003	NOTA ON MIU WRITE WITH EVEN PARITY
0000	0002	NOTA ON MIU WRITE WITH FLIPPER SET
0000	0001	NOTA ON MIU WRITE

Figure 17. Valid Error Displays for Failure of Normal Trace Setup for CRBTST.

00159

```
I* X-RAY
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0 BIU COPY SELECT
0000 8100 - (Default is BIU copy 0)
          -  4100 = BIU COPY 1
X-PARAM ADDR = 1 SPARE

X-PARAM ADDR = 2 PCDC DISPLAY
0002 0001 - (Default is PCDC display)
          -  0000 = NO PCDC DISPLAY

X-PARAM ADDR = 3 ROUTINE MODE
0003 0000 - (Default is DO NOT ROUTINE)
          -  FFFF = ROUTINE
```

Figure 18a. Parameter Control.

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - (Default all phase to be executed)
          -  8000 = PHASE 0 ONLY
          -  4000 = PHASE 1 ONLY
          -  2000 = PHASE 2 ONLY
          -  1000 = PHASE 3 ONLY
          -  0800 = PHASE 4 ONLY
          -  0400 = PHASE 5 ONLY
```

Figure 18b. Phase Selection.

Figure 18. Typical MTCTST Parameter Control, Phase Selection, and Execution.

00160

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF -
          CC00
0001 E600 -
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00050000  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  0016    00007   00005   0   00050000
0002          00024   00007   0   00050000
0003          00301   00201   0R      0800

**MONITOR** V1.2
I* X-RAY
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 CC00 -
           2000
0001 E600 -
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00050000  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  004F    00007   00005   0   00050000
0002          00024   00007   0   00050000
0003          0027C   00022   0L  0005

**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 2000 -
          1000
0001 E600 -
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00050003  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  004F    00007   00005   0   00050003
0002          00024   00007   0   00050003
0003          0027C   00022   0L  0005
```

Figure 18c. Execution.

Figure 18. Typical MTCTST Parameter Control, Phase Selection, and Execution (Continued).

00161

G REGO PHASE	G REGO ERROR NUMBER	FAILING FUNCTION
XXXX	OFFD	CLOCK ERROR
XXXX	OFFE	SYNC ERROR
XXXX	OFFF	CP MASTER ERROR
0000	0001	L MATCH TX TEST - MATCH ERRORS NOT RESET (REF REG 1; - LMATCH, RMATCH, AMATCH, BMATCH)
0000	0002	L MATCH TX TEST - "TX" MATCH ERROR NOT DETECTED (REG 1; - LMATCH, RMATCH ERRORS)
0000	0008	L MATCH TX TEST - "NOTA" ON BIU STATUS WRITE
0001	0001	R MATCH TX TEST - MATCH ERRORS NOT RESET
0001	0002	R MATCH TX TEST - TX MATCH ERROR NOT DETECTED (REG 1; - RMATCH, LMATCH ERRORS)
0001	0008	R MATCH TX TEST - "NOTA" ON BIU STATUS WRITE
0002	0003	L MATCH TEST - COMMAND BUS 1R AND OR "TX" SIGNAL NOT STRAPPED ON BACKPLANE
0002	0004	L MATCH TEST - "COM" SIGNAL MATCH ERROR NOT DETECTED (REG 1; - LMATCH, RMATCH)
0002	0005	L MATCH TEST - FLIPPED BIT MATCH ERROR NOT DETECTED (REG 1; - LMATCH, RMATCH)
0002	0006	L MATCH TEST - PARITY MATCH ERROR NOT DETECTED (REG 1; - LMATCH, RMATCH)
0002	0007	L MATCH TEST - DATA BIT MATCH ERROR NOT DETECTED (REG 1; - LMATCH, RMATCH) REG1 = TEST POINT INDICATORS REG2 = EXPECTED DATA REG3 = ACTUAL DATA REG5 = LAST BUS COMMAND
0002	0008	L MATCH TEST - "NOTA" ON BIU STATUS WRITE
0003	0003	R MATCH TEST - COMMAND BUS 1L AND OL "TX" SIGNAL NOT STRAPPED ON BACKPLANE
0003	0004	R MATCH TEST - "COM" SIGNAL MATCH ERROR NOT DETECTED (REG 1; - RMATCH, LMATCH)
0003	0005	R MATCH TEST - FLIPPED BIT MATCH ERROR NOT DETECTED (REG 1; - RMATCH, LMATCH)
0003	0006	R MATCH TEST - PARITY MATCH ERROR NOT DETECTED (REG 1; - RMATCH, LMATCH)
0003	0008	R MATCH TEST - DATA BIT MATCH ERROR NOT DETECTED (REG 1; - RMATCH, LMATCH)
0003	0008	R MATCH TEST - "NOTA" ON BIU STATUS WRITE
0004	0004	A MATCH TEST - MATCH ERROR DETECTED ON BIU READ
0004	0005	A MATCH TEST - FLIPPER BIT MATCH ERROR NOT DETECTED
0004	0006	A MATCH TEST - PARITY MATCH ERROR NOT DETECTED (REG 1; - AMATCH, BMATCH)
0004	0007	A MATCH TEST - DATA BIT MATCH ERROR NOT DETECTED (REG 1; - AMATCH, BMATCH)
0004	0008	A MATCH TEST - "NOTA" ON BIU WRITE
0004	0009	A MATCH TEST - "NOTA" ON BIU READ

Figure 19. Valid Error Displays for Failure of Normal Trace Setup for MTCTST (Sheet 1 of 2).

REGO		FAILING FUNCTION
PHASE	ERROR NUMBER	
0005	0004	B MATCH TEST - MATCH ERROR DETECTED ON BIU READ
0005	0005	B MATCH TEST - FLIPPER BIT MATCH ERROR NOT DETECTED (REG 1; - BMATCH, AMATCH)
0005	0006	B MATCH TEST - PARITY MATCH ERROR NOT DETECTED (REG 1; - BMATCH, AMATCH)
0005	0007	B MATCH TEST - DATA BIT MATCH ERROR NOT DETECTED (REG 1; - BMATCH, AMATCH)
0005	0008	B MATCH TEST - "NOTA" ON BIU WRITE
0005	0009	B MATCH TEST - "NOTA" ON BIU READ

Figure 19. Valid Error Displays for Failure of Normal Trace Setup for MTCTST (Sheet 2 of 2).

00163

```
I* X-RAY
**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

PCDC DISPLAY = "CDI READY"
INCORRECT VALUE ENTERED = "INVALID ENTRY"
```

TEST NAME	PCDC INPUT	PCDC DISPLAY/RESPONSE
DF KEY CODE TEST	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"45" KEY PAD	DISPLAY = "45"
	DF KEY	DISPLAY = "DF OK"
ASCII CHARACTER INPUT/ECHO	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"00"-"3F" KEY PAD	ENTRY DISPLAYED (REFER TO ASSOCIATED ASCII
	DF KEY	CHARACTER DISPLAYED)
ALPHABETIC CHARACTER DISPLAY	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"40" KEY PAD	DISPLAY = "40"
	DF KEY	DISPLAY =
DECIMAL NUMERIC CHARACTER DISPLAY	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"41" KEY PAD	DISPLAY = "41"
	DF KEY	DISPLAY =
INITALIZATION KEY CODE TEST	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"43" KEY PAD	DISPLAY = "43"
	FORCE AND INIT KEYS	DISPLAY = "INIT OK"
MCS KEY CODE TEST	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"44" KEY PAD	DISPLAY = "44"
	MCS KEY	DISPLAY = "MCS OK"

Figure 20. Typical CDITST Execution (Sheet 1 of 2).

00164

TEST NAME	PCDC INPUT	PCDC DISPLAY/RESPONSE
VARIABLE INPUT FORMATTED DISPLAY	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	ANY CHARACTER REPEATED EIGHT (8) TIMES (XXXXXXXX) EX: "AAAAAAAA"	DISPLAY = INPUT ("XXXXXXXX")
	DF KEY	DISPLAY = FORMATTED INPUT ("XXXX XXXX") EX: "AAAA AAAA"
SOFTWARE COUNTER DISPLAY	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"46" KEY PAD	DISPLAY = "46"
	DF KEY	DISPLAY = SEQUENTIAL SOFTWARE COUNT IN THE FORMAT "00 00"
TERMINATE TEST	START KEY	DISPLAY EXTINGUISHED, START KEY ILLUMINATED
	"DEAD" KEY PAD	DISPLAY = "DEAD"
	CLR KEY	DISPLAY = "TESTING ENDS" X-RAY TRACE DUMP ON SM TERMINAL

Figure 20. Typical CDITST Execution (Sheet 2 of 2).

00165

REG0 = PHASE/ERROR NUMBER
REG1 = INTERNAL TEST POINTS
REG2 = EXPECTED DATA
REG3 = ACTUAL DATA
REG4 = FAIL COUNT/RUN COUNT
REG5 = FUNCTION CODE

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
XXXX	00D0	CLOCK ERROR
XXXX	00E0	SYNC ERROR
0000	00F0	CP MASTER ERROR
0000	0002	CDI REQUEST NOT RECEIVED
0000	0003	CDI REQUEST ON AFTER CDI RESET
0000	0004	CDI NOT READY FOR SENDING
0000	0005	INIT KEY CODE ERROR
0000	0006	MCS KEY CODE ERROR
0000	0007	DF KEY CODE ERROR

Figure 21. Valid Error Displays for Trace Dump During Execution of CDITST Procedure.

00166

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - (Default set to run all phases)
          -  8000 = phase 1 only
          -  4000 = phase 2 only
          -  2000 = phase 3 only
          -  1000 = phase 4 only
          -  0800 = phase 5 only
          -  0400 = phase 6 only
```

Figure 22a. Sequence Control.

Figure 22. Typical MIUTST Sequence Control, Parameter Control, and Execution.

00167

```
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARM ADDR = 0 (MIU's, COPIES, BUS)
0000 FF00 - (Default set for:  MIU's 0,1; COPIES 0,1; BUS 0,1)
          - 8000 = MIU 0 COPY 0 BUS 0
          - 4000 = MIU 0 COPY 0 BUS 1
          - 2000 = MIU 0 COPY 1 BUS 0
          - 1000 = MIU 0 COPY 1 BUS 1
          - 0800 = MIU 1 COPY 0 BUS 0
          - 0400 = MIU 1 COPY 0 BUS 1
          - 0200 = MIU 1 COPY 1 BUS 0
          - 0100 = MIU 1 COPY 1 BUS 1
          - 0080 = MIU 2 COPY 0 BUS 0
          - 0040 = MIU 2 COPY 0 BUS 1
          - 0020 = MIU 2 COPY 1 BUS 0
          - 0010 = MIU 2 COPY 1 BUS 1
          - 0008 = MIU 3 COPY 0 BUS 0
          - 0004 = MIU 3 COPY 0 BUS 1
          - 0002 = MIU 3 COPY 1 BUS 0
          - 0001 = MIU 3 COPY 1 BUS 1

X-PARM ADDR 1 (MIU 0; MU HI/LO UNITS FOR EACH COPY)
0001 2020 - (Default set for; HI MU 2, LO MU 0, COPIES 0,1)
          BITS  0-3  = HI MU COPY 0
          BITS  4-7  = LO MU COPY 0
          BITS  8-11 = HI MU COPY 1
          BITS 12-15 = LO MU COPY 1

X-PARM ADDR = 2 (MIU 1; MU HI/LO UNITS FOR EACH COPY)
0002 2020 - (Default same as MIU0)
          Format same as MIU0

X-PARM ADDR = 3 (MIU 2; MU HI/LO UNITS FOR EACH COPY)
0003 7676 - (Default set for; HI MU7, LO MU6, COPIES 0,1)
          Format same as MIU0

X-PARM ADDR = 4 (MIU 3; MU HI/LO UNITS FOR EACH COPY)
0004 7676 - (Default same as MIU2)
          Format same as MIU0

NOTE:  This program only uses the specified LO MU for addressing and R/W tests.
    It is recommended that for a complete test each MU within the MIU be specified
    as the LO MU.  The program does not test the specified HI MU.
```

Figure 22b. Parameter Control (Sheet 1 of 2).

Figure 22. Typical MIUTST Sequence Control, Parameter Control, and Execution (Continued).

00168

```
X-PARM ADDR = 5 (INITIAL CONFIG OF SUBBUSES, BUSES, MATCHERS)
0005 FFEB - (Default set for; RB1, ALL MATCHERS, CB1, SB 1BL, SB 1AL, SB 0BL, CB0)
          BITS  3 = RESP BUS; 0 = BUS 0, 1 = BUS 1
          BITS  4 = COMMAND MATCHER L; 1 = ENABLE
          BITS  5 = COMMAND MATCHER R; 1 = ENABLE
          BITS  6 = RESPONSE MATCHER A; 1 = ENABLE
          BITS  7 = RESPONSE MATCHER B; 1 = ENABLE
          BITS  9 = COMMAND BUS 1; 1 = DRIVE
          BITS 10 = SUB BUS 1L; 0=A, 1=B
          BITS 11 = SUB BUS 1R; 0=A, 1=B
          BITS 12 = SUB BUS 0L; 0=A, 1=B
          BITS 13 = SUB BUS 0R; 0=A, 1=B
          BITS 15 = COMMAND BUS 0; 1 = DRIVE
```

Figure 22b. Parameter Control (Sheet 2 of 2).

Figure 22. Typical MIUTST Sequence Control, Parameter Control, and Execution (Continued).

00169

```
SECTION 227-200-301
ISSUE 1


X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0

0000 FFFF -

X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARM ADDR = 0

0000 FF00 - FFF0
0001 2020 - 0000
0002 2020 - 0000
0003 7676 - 0000
0004 7676 - 0000
0005 FFEB -

X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
01050000  XXXXXXXX  00000000  A0000003  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  06AA    00007   00005   0   01050000
0002          00033   00007   0   01050000
0003          0029D   0029E   0L  0000
0004          003B0   0029F   0L  8000
0005          0029D   0029E   0L  8000
0006          00269   0026A   0L  0000
0007          00280   00281   2R      0000
0008          0027D   00280   2L  0000
0009          00106   00106   3   A0000003
000A          002FC   002FD   0L  8000
000B          003B1   0012B   2R      8000
000C          002FE   002FF   0L  4000
000D          00106   00106   3   A0000002
000E          002FC   002FD   0L  8000
000F          003B1   00133   2L  8000
0010          002FE   002FF   0L  4000

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
40000000  XXXXXXXX  80008000  A0000002  XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX

**MONITOR** V1.2
```

Figure 22c. Execution.

Figure 22. Typical MIUTST Sequence Control, Parameter Control, and Execution (Continued).

00170

REG0 = TEST, PHASE, ERROR NUMBER
REG1 = INTERNAL TEST POINTS
REG2 = LAST WRITE DATA
REG3 = LAST READ DATA
REG4 = TOTAL FAIL/RUN COUNT
REG5 = LAST BUS COMMAND
REG6 = CURRENT UNIT/UNITS PRESENT
REG7 = MIU 3 HI LO SELECT

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
XXXX	0FFD	CLOCK ERROR
XXXX	0FFE	SYNC ERROR
XXXX	0FFF	NO CP SELECTED MASTER
All of the specified error numbers and explanations apply to any or all of the phases. Refer to detailed error decodes (V, W, X, Y, Z) for specific explanations.		
XXXX	0000	NO RESPONSE TO A DISABLE COMMAND BUT UNIT IS MARKED AS ENABLED
XXXX	0100	NO RESPONSE TO AN ENABLE COMMAND. TWO ENABLE ATTEMPTS WERE MADE IF THE UNIT WAS MARKED AS ENABLED
XXXX	0202	STATUS RESPONSE ERROR DURING ADDRESS RECOGNITION
XXXX	0300	UNIT OTHER THAN REQUESTED RESPONDING TO A READ STATUS COMMAND
XXXX	04YZ	MIU READ ALGORITHM ERROR
XXXX	05XZ	ENABLE/DISABLE ERROR
XXXX	060Z	DISABLED UNIT RESPONDING TO A READ STATUS
XXXX	07VZ	NON-FUNCTIONAL STATUS TEST ERROR
XXXX	08WZ	ACROSS BUS STATUS TEST ERROR

DETAILED ERROR DISPLAY DECODES

V = 0 - BUS ERROR ON NON-FUNCTIONAL DISABLE STATUS WRITE

V = 1 - ENABLED UNIT RESPONDING IMPROPERLY TO A STATUS READ AFTER A NON-FUNCTIONAL STATUS WRITE

V = 2 - NO BUS ERROR ON A NON-FUNCTIONAL ENABLE STATUS WRITE (UNIT IS DISABLED)

V = 3 - DISABLED UNIT RESPONDING TO A STATUS READ AFTER A NON-FUNCTIONAL STATUS WRITE. (WRITE WAS READ/WRITE ENABLED)

V = 4 - BUS ERROR ON READ ENABLE AFTER ACTION 3

Figure 23. Valid Error Displays for Failure of Normal Trace Setup for MIUTST (Sheet 1 of 4).

00171

V = 5 - STATUS RESPONSE ERROR AFTER READ ENABLE ACTION 4

W = 0 - STATUS RESPONSE ERROR ON READ STATUS ON SPECIFIED (CURRENT) BUS

W = 1 - BUS ERROR ON READ ENABLE OF OTHER BUS

W = 2 - STATUS RESPONSE ERROR AFTER READ ENABLE OF OTHER BUS (SHOULD NOT BE READ ENABLED)

W = 3 - BUS ERROR ON WRITE ENABLE OF OTHER BUS

W = 4 - STATUS RESPONSE ERROR AFTER WRITE ENABLE OF OTHER BUS

W = 5 - BUS ERROR ON READ ENABLE OF OTHER BUS ON ITS OWN SIDE

W = 6 - STATUS RESPONSE ERROR AFTER READ ENABLE OF OTHER BUS

W = 7 - BUS ERROR ON NON-FUNCTIONAL DISABLE TO THE OTHER BUS

W = 8 - STATUS RESPONSE ERROR AFTER A NON-FUNCTIONAL DISABLE TO THE OTHER BUS

W = 9 - BUS ERROR ON A WRITE DISABLE OF THE OTHER BUS

W = A - STATUS RESPONSE ERROR AFTER A WRITE DISABLE OF THE OTHER BUS

W = B - BUS ERROR ON A READ DISABLE OF THE OTHER BUS

W = C - STATUS RESPONSE ERROR AFTER A READ DISABLE OF THE OTHER BUS

X = 0 - DISABLED UNIT RESPONDING TO A WRITE COMMAND X = 1 - DISABLED UNIT RESPONDING TO A READ COMMAND

X = 2 - UNIT RESPONDING TO WRITE ENABLE WHEN READ DISABLED

X = 3 - UNIT WRITE ENABLED ONLY RESPONDING TO READ

X = 4 - UNIT WRITE ENABLED ONLY NOT RESPONDING TO WRITE

X = 5 - UNIT NOT RESPONDING TO READ ENABLE

X = 6 - READ ENABLED UNIT NOT RESPONDING TO READ STATUS

X = 7 - READ ENABLED UNIT NOT RESPONDING TO READ DATA

X = 8 - DATA READ FROM PREVIOUS WRITE IS INCORRECT

X = 9 - READ/WRITE ENABLED UNIT NOT RESPONDING TO WRITE

X = A - DATA READ FROM PREVIOUS WRITE IS INCORRECT (ALL 5'S)

X = B - READ/WRITE ENABLED UNIT NOT RESPONDING TO WRITE DISABLE

Figure 23. Valid Error Displays for Failure of Normal Trace Setup for MIUTST (Sheet 2 of 4).

00172

X = C - READ ENABLED/WRITE DISABLED UNIT NOT RESPONDING TO READ DATA

X = D - MEMORY DATA ALTERED FROM LAST ENABLED WRITE

X = E - READ ENABLED UNIT NOT RESPONDING TO READ DISABLE

X = F - READ/WRITE DISABLED UNIT RESPONDING TO MEMORY READ

Y = 0 - COPY 0, BUS 0 RESPONDING WHEN COPY BITS = 00

Y = 1 - COPY 0, BUS 0 RESPONDING WHEN COPY BITS = 01

Y = 2 - COPY 0, BUS 0 NOT RESPONDING WHEN COPY BITS = 10

Y = 3 - COPY 0, BUS 0 NOT RESPONDING WHEN COPY BITS = 11

Y = 4 - COPY 0, BUS 1 RESPONDING WHEN COPY BITS = 00

Y = 5 - COPY 0, BUS 1 RESPONDING WHEN COPY BITS = 01

Y = 6 - COPY 0, BUS 1 NOT RESPONDING WHEN COPY BITS = 10

Y = 7 - COPY 0, BUS 1 RESPONDING WHEN COPY BITS = 11

Y = 8 - COPY 1, BUS 0 RESPONDING WHEN COPY BITS = 00

Y = 9 - COPY 1, BUS 0 NOT RESPONDING WHEN COPY BITS = 01

Y = A - COPY 1, BUS 0 RESPONDING WHEN COPY BITS = 10

Y = B - COPY 1, BUS 0 RESPONDING WHEN COPY BITS = 11

Y = C - COPY 1, BUS 1 RESPONDING WHEN COPY BITS = 00

Y = D - COPY 1, BUS 1 NOT RESPONDING WHEN COPY BITS = 01

Y = E - COPY 1, BUS 1 RESPONDING WHEN COPY BITS = 10

Y = F - COPY 1, BUS 1 NOT RESPONDING WHEN COPY BITS = 11

Z = 0 - NO RESPONSE

Z = 1 - COPY AND MIU ID IN STATUS WORD MISMATCH WITH COMMAND

Z = 2 - BUS 0 NOT MARKED AS READ ENABLED

Z = 3 - BUS 0 NOT MARKED AS WRITE ENABLED

Figure 23. Valid Error Displays for Failure of Normal Trace Setup for MIUTST (Sheet 3 of 4).

00173

Z = 4 - BUS 0 NOT MARKED AS READ DISABLED

Z = 5 - BUS 0 NOT MARKED AS WRITE DISABLED

Z = 6 - BUS 1 NOT MARKED AS READ ENABLED

Z = 7 - BUS 1 NOT MARKED AS WRITE ENABLED

Z = 8 - BUS 1 NOT MARKED AS READ DISABLED

Z = 9 - BUS 1 NOT MARKED AS WRITE DISABLED

Figure 23. Valid Error Displays for Failure of Normal Trace Setup for MIUTST (Sheet 4 of 4).

00174

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - (Default set for all phases to run)
          - 8000 = PHASE 0 ONLY
          - 4000 = PHASE 1 ONLY
          - 2000 = PHASE 2 ONLY
          - 1000 = PHASE 3 ONLY
          - 0800 = PHASE 4 ONLY
          - 0400 = PHASE 5 ONLY
          - 0200 = PHASE 6 ONLY
```

Figure 24a. Phase Select Control.

Figure 24. Typical MUTEST Phase Select Control, Parameter Control, and Execution.

00175

```
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARM ADDR = 0 (MIU 0; MU 0-7 COPY 0, MU 0-7 COPY 1)
0000 E0E0 - (Default set for MIU0, MU 0-2 COPY 0 & 1)
          - 8000 = MU 0 COPY 0
          - 4000 = MU 1 COPY 0
          - 2000 = MU 2 COPY 0
          - 1000 = MU 3 COPY 0
          - 0800 = MU 4 COPY 0
          - 0400 = MU 5 COPY 0
          - 0200 = MU 6 COPY 0
          - 0100 = MU 7 COPY 0
          - 0080 = MU 0 COPY 1
          - 0040 = MU 1 COPY 1
          - 0020 = MU 2 COPY 1
          - 0010 = MU 3 COPY 1
          - 0008 = MU 4 COPY 1
          - 0004 = MU 5 COPY 1
          - 0002 = MU 6 COPY 1
          - 0001 = MU 7 COPY 1


X-PARAM ADDR = 1 (MIU1; MU 0-7 COPY 0, MU 0-7 COPY 1)
0001 E0E0 - (Default same as MIU0)
          Format same as MIU0


X-PARAM ADDR = 2 (MIU2; MU 0-7 COPY 0, MU 0-7 COPY 1)
0002 0000 - (Default set for no MU's)
          Format same as MIU0


X-PARAM ADDR = 3 (MIU3; MU 0-7 COPY 0, MU 0-7 COPY 1)
0003 0000 - (Default set for no MU's)
          Format same as MIU0


X-PARAM ADDR = 4 (PCDC Display of current unit under test)
0004 0000 - (Default set for No PCDC display)
          - FFFF = PCDC Display


X-PARAM ADDR = 5 (Routine Control)
0005 0000 - (Default set for No routine-Normal Execution)
          - FFFF = Routine
```

Figure 24b. Parameter Control.

Figure 24. Typical MUTEST Phase Select Control, Parameter Control, and Execution (Continued).

00176

```
X-RAY (S,L,E,EM,I,T,P,C) = E (Normal Execution)

I* RESTART
**MONITOR**
(Wait for program to complete current run)
  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
                                          ERR/RUN
                                          CNT/CNT
X-RAY (S,L,E,EM,I,TP,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF -

X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0

0000 E0E0 - FCFC
0001 E0E0 - FCFC
0002 0000 - FCFC
0003 0000 - /
0004 0000 - z
0005 0000 -

X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000001  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  013F    00007   00005   0   00000000
0002          0003F   00007   4   00000001
0003          0003E   00040   0L  0000
0004          00074   0003B   0L  463F
0005          0031F   00071   0L  0007
0006          00090   0006E   0L  0006
0007          00319   0006B   0L  0005
0008          00312   00068   0L  0004
0009          0030C   00065   0L  0003
000A          00083   00062   0L  0002
000B          00336   0005F   0L  0001
000C          0003B   00075   0L  4A00
000D          0031F   00071   0L  0007
000E          00090   0006E   0L  0006
000F          00319   0006B   0L  0005
0010          00312   00068   0L  0004

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00040000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000001  XXXXXXXX  XXXXXXXX  XXXXXXXX
```

Figure 24c. Execution (Sheet 1 of 2).

Figure 24. Typical MUTEST Phase Select Control, Parameter Control, and Execution (Continued).

00177

```
I* RESTART

**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000005  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  0012    00007   00005   0   00000000
0002          0003F   00007   4   00000005
0003          0003E   00040   0L  0000
0004          00042   0003B   0L  463F
0005          0003A   00040   0L  0000
0006          00042   00037   0L  4A3F
0007          00036   00040   0L  0000
```

Figure 24c. Execution (Sheet 2 of 2).

Figure 24. Typical MUTEST Phase Select Control, Parameter Control, and Execution (Continued).

00178

REG0 = PHASE/ERROR NUMBER
REG1 = INTERNAL TEST POINTS
REG2 = EXPECTED DATA
REG3 = ACTUAL DATA
REG4 = RUN COUNT/ERROR COUNT
REG5 = LAST BUS COMMAND
REG6 = MIU 0 & 1 MU'S EQUIPPED (PARAM-ADDR = 0 & 1)
REG7 = MIU 2 & 3 MU'S EQUIPPED (PARAM-ADDR = 2 & 3)

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
0000	0FFD	CLOCK ERROR
0000	0FFE	SYNC ERROR
0000	0FFF	NO CP SELECTED MASTER
0000	0001	PARITY, NOTA, NOTX, DATA TO, OR DATA LOST ON MIU STATUS READ
0000	0002	INCORRECT STATUS FROM MIU STATUS READ
0001	0003	NOTA OR NOTX ON MEMORY WRITE WITH DATA EVEN PARITY
0001	0004	PARITY ERROR NOT DETECTED ON MEMORY READ
0002	0005	NOTA OR NOTX ON MEMORY WRITE OF ALL 0'S
0002	0006	PARITY ERROR ON MEMORY READ OF ALL 0'S
0002	0007	NOTA, NOTX, DATA TO OR DATA LOST ON MEMORY READ (ALL 0'S)
0002	0008	PARITY BIT NOT DETECTED ON MEMORY READ OF ALL 0'S
0002	000D	DATA MISMATCH ON MEMORY READ - ALL 0'S
0003	0005	NOTA, OR NOTX ON MEMORY WRITE OF ALL 1'S
0003	0006	PARITY ERROR ON MEMORY READ OF ALL 1'S
0003	0007	NOTA, NOTX, DATATO, OR DATA LOST ON MEMORY READ - ALL 1'S
0003	0008	PARITY BIT NOT DETECTED ON MEMORY READ - ALL 1'S
0003	000D	DATA MISMATCH ON MEMORY READ - ALL 1'S
0004	0005	NOTA, OR NOTX ON MEMORY ADDRESS WRITE
0004	0006	PARITY ERROR ON MEMORY ADDRESS READ
0004	0007	NOTA, NOTX, DATA TO, OR DATA LOST ON MEMORY ADDRESS READ
0004	000D	DATA MISMATCH ON MEMORY ADDRESS READ
0005	0005	NOTA, OR NOTX ON MEMORY WRITE OF EACH BIT POSITION
0005	0006	PARITY ERROR ON MEMORY READ OF EACH BIT POSITION
0005	0007	NOTA, NOTX, DATA TO OR DATA LOST ON MEMORY READ OF EACH BIT
0005	0009	PARITY BIT DETECTED ON MEMORY READ OF EACH BIT POSITION
0005	000D	DATA MISMATCH ON MEMORY READ OF EACH BIT POSITION

Figure 25. Valid Error Displays for Failure of Normal Trace Setup for MUTEST (Sheet 1 of 2).

00179

REGO PHASE	REGO ERROR NUMBER	FAILING FUNCTION
0006	0005	NOTA, OR NOTX ON MEMORY WRITE WITH FLIPPER AND ALL 0'S
0006	0006	PARITY ERROR ON MEMORY READ OF FLIPPER AND ALL 1'S
0006	0007	NOTA, NOTX, DATA TO, OR DATA LOST ON MEMORY READ WITH FLIPPER AND ALL 1'S
0006	000A	FLIPPER BIT NOT SET ON MEMORY READ OF FLIPPER AND ALL 1'S
0006	000B	DATA MISMATCH ON MEMORY READ (ALL 0'S FLIPPER TO ALL 1'S)
0007	0005	NOTA OR NOTX ON MEMORY WRITE WITH FLIPPER AND ALL 1'S
0007	0006	PARITY ERROR ON MEMORY READ OF FLIPPER AND ALL 0'S
0007	0007	NOTA, NOTX, DATA TO, DATA LOST ON MEMORY READ WITH FLIPPER AND ALL 0'S
0007	000A	FLIPPER BIT NOT SET ON MEMORY READ OF FLIPPER AND ALL 0'S
0007	000B	DATA MISMATCH ON MEMORY READ (ALL 1'S FLIPPER TO ALL 1'S)
XXXX	000C	FLIPPER BIT SET ON MEMORY READ WHEN NOT INTENDED

Figure 25. Valid Error Displays for Failure of Normal Trace Setup for MUTEST (Sheet 2 of 2).

REG OL	BIU COPY	CMD BUS	RESP BUS	DSRB	BIU BUS PRT	TEST
8100	0	0	0	SET	0	A - SHOULD BE UNREADABLE (-NOTA)
8100	0	1	1	SET	0	B - STATUS DSRB SET ON PROPER BUS
8100	0	1	1	SET	0	C - STATUS DSRB NOT SET ON OTHER BUS
8100	0	1	1	RESET	0	D - SHOULD NOT ENABLE
8100	0	0	0	RESET	0	E - SHOULD BE READABLE
8100	0	0	0	RESET	0	F - STATUS DSRB RESET
8100	0	1	1	SET	0	G - STATUS OF DSRB ON OTHER BUS RESET
8100	0	0	0	RESET	0	H - INITIALIZE
8100	0	1	1	SET	1	A - SAME AS ABOVE
8100	0	0	0	SET	1	B - SAME AS ABOVE
8100	0	0	0	SET	1	C - SAME AS ABOVE
8100	0	0	0	RESET	1	D - SAME AS ABOVE
8100	0	1	1	RESET	1	E - SAME AS ABOVE
8100	0	1	1	RESET	1	F - SAME AS ABOVE
8100	0	0	0	SET	1	G - SAME AS ABOVE
8100	0	1	1	RESET	1	H - SAME AS ABOVE
8100	1	0	0	SET	0	A - SAME AS ABOVE

NOTE: The above sequence is repeated for BIU copy 1.

Figure 26. SRB Status Tests.

00181

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - (Default set to run all phases)
          - 8000 = RUN PC MAP TEST ONLY
          - 4000 = RUN BIU SRB STATUS TEST ONLY
```

Figure 27a. Phase Select.

```
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
41000400  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  000E000E

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  000B    00007   00005   7   000E000E
0002          0001A   00007   7   00050005
0003          0001A   000C0   0L  4100
0004          0008E   0008F   0R      0400
0005          0002B   0008E   0L  8100
0006          0005A   00035   0L  4100
0007          0002B   0002E   0L  8100
0008          00002   0000E   0   00000000
0009          00001   00001   4   00000000
000A          00001   00001   7   00010001
000B          00000   00000   7   00010001

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  00010001

**MONITOR** V1.2
```

Figure 27b. Execution.

Figure 27. Typical BIUTST Phase Select and Execution.

00182

REG0 = BIU BUS COMMAND WORD (SRA8)

NOTE: This program does not utilize phase number in REG0.

REG1 = INTERNAL TEST POINTS
REG2 = EXPECTED DATA (SRA11)
REG3 = ACTUAL DATA
REG4 = FAIL COUNT/RUN COUNT (NOT USED)
REG5 = LAST BUS COMMAND (SRA10)
REG6 = RESPONSE BUS READ DATA (RA12)

REG0		REG5	
BIU BUS CMD	ERROR NUMBER	LAST CMD	FAILING FUNCTION
XXXX	00D0	XXXX	CLOCK ERROR
XXXX	00E0	XXXX	SYNC ERROR
XXXX	00F0	XXXX	NO CP SELECTED MASTER
XXXX	0001	C1000400	NOTX OR NOTA ON BIU STATUS WRITE MAP
8100	0002	8183EXXX	DATA MISMATCH - PC MAP TEST BIU0 MAP
4100	0002	4183EXXX	DATA MISMATCH - PC MAP TEST BIU1
8100	0002	81800400	PARITY ERROR ON BIU0 READ - DSRB TEST
4100	0002	41800400	PARITY ERROR ON BIU1 READ - DSRB TEST
8100	0003	8180XXXX	NOTX, NOTA, DATATO, OR DATALOST BIU0 READ
4100	0003	4180XXXX	NOTX, NOTA, DATATO, OR DATALOST BIU1 READ
8100	0004	8180XXXX	RESPONSE (-NOTA) FROM BIU0 WITH DSRB SET
4100	0004	4140XXXX	RESPONSE (-NOTA) FROM BIU1 WITH DSRB SET

REG0		REG6	
BIU BUS CMD	ERROR NUMBER	RESP BUS DATA	FAILING FUNCTION
8100	0005	02X0XXXX	DSRB NOT SET ON DISABLED BUS-BIU0, BUS0
4100	0005	01XX00X0	DSRB NOT SET ON DISABLED BUS-BIU1, BUS1
8100	0006	02X1XXXX	DSRB SET ON OPPOSITE BUS-BIU0, BUS0
4100	0006	01XX00X1	DSRB SET ON OPPOSITE BUS-BIU1, BUS1
8100	0007	02X0XXXX	DSRB RESET VIA OPPOSITE BUS-BIU0, BUS1
4100	0007	01XX00X0	DSRB RESET VIA OPPOSITE BUS-BIU1, BUS0
8100	0008	02X1XXXX	DSRB NOT RESET VIA SAME BUS-BIU0, BUS0
4100	0008	01XX00X1	DSRB NOT RESET VIA SAME BUS-BIU1, BUS1
8100	0009	02X0XXXX	DSRB NOT SET VIA OPPOSITE BUS-BIU0, BUS0
4100	0009	01XX00X0	DSRB NOT SET VIA OPPOSITE BUS-BIU1, BUS1

Figure 28. Valid Error Displays for Failure of Normal Trace Setup for BIUTST.

00183

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - Default = RUN ALL PHASES
          - 8000 = PHASE 0
          - 4000 = PHASE 1
          - 2000 = PHASE 2
          - 1000 = PHASE 3
          - 0800 = PHASE 4
```

Figure 29a. Phase Select.

```
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0 BIU/BUS COPY SELECT
0000 F000 - Default = BIU0,1; BUS 0
          - 8000 = BIU 0, BUS 0
          - 4000 = BIU 0, BUS 1
          - 2000 = BIU 1, BUS 0
          - 1000 = BIU 1, BUS 1

X-PARAM ADDR = 1 PC PAGE SELECT
0001 0000 - Default = PC PAGE 0 (Bits 14-15)

X-PARAM ADDR = 2 PCU, MATRIX, CODE, WORD SELECT
0002 001F - Default = PCU0, MATRIX0, CODE0, WORD31
          - 061F = PCU 0, MATRIX 6, CODE 0, WORD 31
          - 071F = PCU 0, MATRIX 7, CODE 0, WORD 31

X-PARAM ADDR = 3 ROUTINE MODE
0003 0000 - Defauot = DO NOT ROUTINE
          - FFFF = ROUTINE
```

Figure 29b. Parameter Control.

Figure 29. Typical PAUTST Phase Select, Parameter Control, and Execution.

00184

```
SECTION 227-200-301
ISSUE 1


X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0       REG1       REG2       REG3       REG4       REG5       REG6       REG7
00070000   XXXXXXXX   XXXXXXXX   XXXXXXXX   00000001   XXXXXXXX   XXXXXXXX   XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  002A    00007   00005   0   00070000
0002          00031   00007   4   00000001
0003          000E0   000D0   0L  0007
0004          000E0   000CB   0L  0006
0005          000DC   000C4   0L  0005
0006          000BA   0004F   0L  0004
0007          000A3   0004D   0L  0003
0008          0008B   0004B   0L  0002
0009          000DC   00049   0L  0001
000A          00035   00036   0L  C000
000B          000E0   000D0   0L  0007
000C          000E0   000CB   0L  0006
000D          000DC   000C4   0L  0005
000E          000BA   0004F   0L  0004
000F          000A3   0004D   0L  0003
0010          0008B   0004B   0L  0002

  REG0       REG1       REG2       REG3       REG4       REG5       REG6       REG7
00020000   XXXXXXXX   XXXXXXXX   XXXXXXXX   00000001   XXXXXXXX   XXXXXXXX   XXXXXXXX

**MONITOR** V1.2
```

Figure 29c. Execution.

Figure 29. Typical PAUTST Phase Select, Parameter Control, and Execution (Continued).

00185

REG7 = CURRENT CONFIGURATION
REG6 = ACTUAL BUS COMMAND
REG5 = LAST BUS COMMAND
REG4 = FAIL COUNT AND RUN COUNT
REG3 = ACTUAL DATA
REG2 = EXPECTED DATA
REG1 = INTERNAL TEST POINTS
REG0 = PHASE AND ERROR NUMBER

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
0000	0FFD	CLOCK ERROR
0000	0FFE	SYNC ERROR
0000	0FFF	NO CP SELECTED MASTER
0000	0002	NOTA ON STATUS WRITE
0001	0001	PARITY ERROR ON PAU RTN FOR PC STATUS
0001	0002	NOTA, NOTX, DATA TO, OR DATA LOST ON PAU RTN FOR PC STATUS
0001	0004	ADDRESS ECHO MISMATCH ON PC STATUS
0001	0008	DATA RTN NOT ZERO ON PC STATUS WRITE
0002	0001	PARITY ERROR ON PAU RTN FOR PC DATA REG
0002	0002	NOTA, NOTX, DATA TO, OR DATA LOST ON PAU RTN FOR PC DATA REG
0002	0004	ADDRESS ECHO MISMATCH ON PC DATA REG
0002	0005	DATA ECHO MISMATCH ON PC DATA REG
0002	0006	ACTUAL/EXPECTED DATA MISMATCH FOR PC DATA REG
0003	0001	PARITY ERROR ON PAU RTN FOR PU DATA REG
0003	0002	NOTA, NOTX, DATA TO, OR DATA LOST ON PAU RTN
0003	0004	ADDRESS ECHO MISMATCH ON PU DATA REG
0003	0005	DATA ECHO MISMATCH ON PU DATA REG
0003	0006	ACTUAL/EXPECTED DATA MISMATCH ON PU DATA REG
0004	0002	NOTA ON BIU STATUS WRITE
0004	0007	-NOTA ON NORMAL PC R/W WITH DWRT SET

Figure 30. Valid Error Displays for Failure of Normal Trace Setup for PAUTST.

00186

```
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0 PC COPY
0000 8000 - Default = PC COPY 0
          - 4000 = PC COPY 1

X-PARAM ADDR = 1 PC UNIT
0001 0000 - Default = PCU0, MATRIX0, CODE0, WORD0
          - 0600 = PCU0, MATRIX6, CODE0, WORD0
          - 0700 = PCU0, MATRIX7, CODE0, WORD0
```

Figure 31a. Parameter Control Selection.

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 F000 - Default = RUN PHASES 0,1,2,3 ONLY
          - 8000 = RUN PHASE 0 ONLY
          - 4000 = RUN PHASES 0,1 ONLY
          - 2000 = RUN PHASES 0,2 ONLY
          - 1000 = RUN PHASES 0,3 ONLY
          - 0800 = RUN PHASES 0,4 ONLY
```

Figure 31b. Phase Selection.

Figure 31. Typical PAUTST Parameter Control Selection, Phase Selection, and Execution.

00187

```
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00030000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  0010    00007   00005   0   00030000

**MONITOR** V1.2

I* X-RAY

**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0

0000 F000 -
          0800
0001 E600

X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00030000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  0011    00007   00005   0   00030000

**MONITOR** V1.2

I* X-RAY

**X-RAY**
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0

0000 0800 -
          1000
0001 E6000 -

X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00030000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA
0001  0011    00007   00005   0   00030000
```

Figure 31c. Execution.

Figure 31. Typical PAUTST Parameter Control Selection, Phase Selection, and Execution (Continued).

00188

REG7 = CURRENT CONFIGURATION
REG6 = PREVIOUS COMMAND (WPU OR RPU)
REG5 = LAST BUS COMMAND
REG4 = FAIL COUNT AND RUN COUNT
REG3 = ACTUAL DATA
REG2 = EXPECTED DATA
REG1 = INTERNAL TEST POINTS
REG0 = TEST, PHASE, AND ERROR NUMBER

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
0000	0FFD	CLOCK ERROR
0000	0FFE	SYNC ERROR
0000	0FFF	NO CP SELECTED MASTER
0000	0002	NOTX OR NOTA ON BIU STATUS WRITE
0001	0002	NOTA ON PAU WRITE
0002	0001	PARITY ERROR ON PAU READ
0002	0002	NOTA, NOTX, DATATO OR DATA LOST ON PAU READ
0002	0004	ADDRESS ECHO MISMATCH
0003	0001	PARITY ERROR ON PAU READ
0003	0002	NOTA, NOTX, DATA TO OR DATA LOST ON PAU READ
0003	0005	DATA ECHO NOT ZERO (0)
XX00	0001	PARITY ERROR ON PAU OPERATION
XX00	0002	NOTA, NOTX, DATA TO, OR DATA LOST ON PAU OPERATION
XX00	0004	ADDRESS ECHO MISMATCH
XX00	0005	DATA ECHO MISMATCH
XX00	0D00	NO RESPONSE FROM CDI/PCDC
0100	0006	PC WORD ONE (1) NOT RESET ON MASTER CLEAR
0200	0007	FIFO DATA MISMATCH
0300	000F	READ TAPE NOT LOADED - PCDC DISPLAY
0400	000F	WRITE TAPE NOT LOADED - PCDC DISPLAY
0400	0008	MTU INPUT NOT READY
0400	0009	MAG TAPE DATA MISMATCH
0400	000A	MAG TAPE PARITY ERROR ON READ
0400	000B	MTU OUTPUT NOT READY
0400	000C	MAG TAPE PARITY ERROR ON WRITE

Figure 32. Valid Error Displays for Failure of Normal Trace Setup for MTUTST.

00189

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 C000 - Default = RUN BOTH PHASES AND CDI/PCDC EQUIPPED
          - 8000 = RUN GENERAL REGISTER TEST
          - 4000 = RUN NEPC TEST
          - XXX1 = CDI/PCDC NOT EQUIPPED
```

Figure 33a. Phase Select.

```
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX  55555555  AAAAAAAA  55555555  XXXXAAAA

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  0800    00007   00005   0   00000000
0002          00052   00007   0   00000000
0003          00108   00168   7R      AAAA
0004          00108   00108
0005          00168   00108   6L  5555
0006          00168   00168
0007          00108   00168   6R      5555
0008          00108   00108
0009          00168   00108   5L  AAAA
000A          00168   00168
000B          00108   00168   5R      AAAA
000C          00108   00108
000D          00168   00108   4L  5555
000E          00168   00168
000F          00108   00168   4R      5555
0010          00108   00108

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX  55555555  AAAAAAAA  55555555  XXXXAAAA

**MONITOR** V1.2
```

Figure 33b. Execution.

Figure 33. Typical GRNEPCTST Phase Select and Execution.

00190

REG7 = NOT USED
REG6 = MEMORY ADDRESS
REG5 = LAST BUS COMMAND
REG4 = FAIL COUNT AND RUN COUNT
REG3 = ACTUAL DATA
REG2 = EXPECTED DATA
REG1 = INTERNAL TEST POINTS
REG0 = PHASE AND ERROR NUMBER

REG0		FAILING FUNCTION
PHASE	ERROR NUMBER	
0000	00FF	NO TEST SELECTED
0000	00E0	SYNC CLOCK ERROR
0000	00D0	CLOCK ERROR
0000	0008	NO CP SELECTED MASTER
0000	0007	NO RESPONSE FROM CDI
0000	0009	NOTA ON MIU WRITE STATUS (MIU0, CPY0)
0000	0001	NOTA ON MEMORY WRITE OF MACRO INSTRUCTION
0000	0002	NOTA ON MEMORY WRITE OF MACRO INSTRUCTION
0000	0003	NOTA ON MEMORY WRITE OF LAST INSTRUCTION
0000	0004	INSTRUCTION DECODE TRAP 00 MAP ERROR
0000	0005	NO INSTRUCTION DECODE
0000	0006	NOTA ON MEMORY WRITE OF TPR INSTRUCTION
0000	000A	NOTA ON MEMORY INITIALIZATION - ALL 0'S

Figure 34. Valid Error Displays for Failure of Normal Trace Setup for GRNEPCTST.

00191

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 FFFF - Default = Run all phases
          - 8000 = PHASE 0 ZERO MEMORY
          - 4000 = PHASE 1 STACK DATA TEST
          - 2000 = PHASE 2 STACK ADDRESSING TEST
          - 1000 = PHASE 3 IAR TEST
          - 0800 = PHASE 4 NEXT FETCH COUNTER TEST
          - 0400 = PHASE 5 SELF INTERRUPT COUNTER TEST
          - 0200 = PHASE 6 IREG TEST POINT TEST
          - 0100 = PHASE 7 VFLAG TEST
          - 0080 = PHASE 8 BMG TEST
```

Figure 35a. Phase Selection.

```
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0 EQUIPPED MEMORY
0000 2200 - Default = MIU0 COPY0, MU0
          - 2100 = MIU 0, COPY 1, MU 0
          - 1220 = MIU 1, COPY 0, MU 1
          - 1104 = MIU 1, COPY 1, MU 1
          - 0A10 = MIU 2, COPY 0, MU 2
          - 0902 = MIU 2, COPY 1, MU 2
          - 0638 = MIU 3, COPY 0, MU 7
          - 0507 = MIU 3, COPY 1, MU 7

X-PARAM ADDR = 1 ROUTINE MODE
0001 0000 - Default = NO ROUTINING
          - FFFF = ROUTINING
```

Figure 35b. Parameter Control.

Figure 35. Typical STKTST Phase Selection, Parameter Control, and Execution.

00192

```
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00080000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  0800    00007   00005   0   00080000
0002          00042   00007   4   00000000
0003          00210   00040   0L  0008
0004          000CD   0003E   0L  0007
0005          000B0   0003C   0L  0006
0006          00250   0003A   0L  0005
0007          000A8   00038   0L  0004
0008          000A9   0008E
0009          000A9   0008E
000A          000A9   0008E
000B          000A9   0008E
000C          000A9   0008E
000D          000A9   0008E
000E          000A9   0008E
000F          000A9   0008E
0010          000A9   0008E

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00040000  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  XXXXXXXX  XXXXXXXX  XXXXXXXX

**MONITOR** V1.2
```

Figure 35c. Execution.

Figure 35. Typical STKTST Phase Selection, Parameter Control, and Execution (Continued).

00193

REGO PHASE	ERROR NUMBER	FAILING FUNCTION
0000	OFFD	CLOCK ERROR
0000	OFFE	SYNC ERROR
0000	OFFF	NO CP SELECTED MASTER
0000	0005	ERROR (INTR1) ON MIU STATUS WRITE
0000	0006	ERROR (INTR1) ON MEMORY WRITE INITIALIZATION ALL 0'S
0001-3, 5,6,8	0001	ERROR (INTR1) ON MEMORY WRITE DATA PATTERNS
0001-3, 5,6,7	0002	ERROR (INTR1) ON DECODE
0001-3, 5,6,7	0003	MEMORY DATA MISMATCH
0001-3, 5,6,7	0004	DECODE VECTOR NOT TAKEN
0004	0001	NEXT FETCH COUNTER ADDRESS MISMATCH
0004	0002	NEXT FETCH COUNTER ADDRESS DID NOT INCREMENT
0004	0003	NEXT FETCH COUNTER NOT ZERO
0007	0001	VFLAG NOT RESET
0007	0002	VFLAG NOT SET
0007	0003	COPY 00 ERROR
0007	0004	DATALOST ERROR
0007	0005	DATATO ERROR

Figure 36. Valid Error Displays for Failure of Normal Trace Setup for STKTST.

00194

```
X-RAY (S,L,E,EM,I,T,P,C) = C
X-SEQNCE ADDR = 0
0000 8000 - Default = STOP ON FIRST ERROR, CDI/PCDC EQUIPPED
          - 4000 = ATTEMPT ALL VECTORS AND REPORT ERROR COUNT,
                   CDI/PCDC EQUIPPED
          - 1000 = CDI/PCDC NOT EQUIPPED
          - XOYZ
              X = DON'T CARD
              Y = MOST SIGNIFICANT BYTE OF STOP ERROR VECTOR NUMBER
                  1-"FF"
              Z = LEAST SIGNIFICANT BYTE OF STOP ERROR VECTOR NUMBER
                  1-"FF"
```

Figure 37a. Error Reporting Parameter Selection.

```
X-RAY (S,L,E,EM,I,T,P,C) = P
X-PARAM ADDR = 0 MIU SELECTION FOR MACRO STORAGE
0000 2200 - Default = MIU0, COPY0, MU0
          - 2100 = MIU 0, COPY 1, MU 0
          - 1220 = MIU 1, COPY 0, MU 1
          - 1104 = MIU 1, COPY 1, MU 1
          - 0A10 = MIU 2, COPY 0, MU 2
          - 0902 = MIU 2, COPY 1, MU 2
          - 0638 = MIU 3, COPY 0, MU 7
          - 0507 = MIU 3, COPY 1, MU 7

X-PARAM ADDR = 1 FIRST MEMORY LOCATION FOR MACRO STORAGE
0001 0010 - Default = LOCATION "10"
          - 00FF = LOCATION "FF"
```

Figure 37b. Parameter Control.

Figure 37. Typical DCDTST Error Reporting Parameter Selection, Parameter Control, and Execution.

00195

```
X-RAY (S,L,E,EM,I,T,P,C) = E
**MONITOR** V1.2

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00020000  XXXXXXXX  XXXX0200  XXXX01FF  XXXXXXXX  XXXX00E7  1B070000  XXXXXXXX

LINE  EVENTS  FR-ADR  TO-ADR  GR  GR-DATA

0001  053F    00007   00005   0   00020000
0002          0003D   00007   0   00020000
0003          00065   00063   0R      0000
0004          0005D   0005E   5R      00E7
0005          000AD   0005D   2R      0200
0006          000AB   000AC   3R      01FF
0007          000AA   000AB   2R      01FF
0008          000A9   000AA   6   1B070000
0009          00098   000A5
000A          0005D   0005E   5R      00E6
000B          000AD   0005D   2R      01FF
000C          000AB   000AC   3R      01FE
000D          000AA   000AB   2R      01FE
000E          000A9   000AA   6   1BF7FF0F
000F          00098   000A5
0010          0005D   0005E   5R      00E5

  REG0      REG1      REG2      REG3      REG4      REG5      REG6      REG7
00020000  XXXXXXXX  XXXX01FE  XXXX01FE  XXXXXXXX  XXXX00E5  1BF7FF0F  XXXXXXXX

**MONITOR** V1.2

I* XR
```

Figure 37c. Execution.

Figure 37. Typical DCDTST Error Reporting Parameter Selection, Parameter Control, and Execution (Continued).

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REG7 = MIU AND FIRST MEMORY LOCATION SELECTED
REG6 = LAST MACRO INSTRUCTION EXECUTED
REG5 = LAST MEMORY LOCATION OF MACRO INSTRUCTION
REG4 = ERROR STOP AND LAST FAIL COUNT
REG3 = LAST ACTUAL VECTOR LOCATION
REG2 = LAST EXPECTED VECTOR LOCATION
REG1 = INTERNAL TEST POINTS
REG0 = PHASE AND ERROR NUMBER

REG0		
PHASE	ERROR NUMBER	FAILING FUNCTION
0000	00D0	CLOCK ERROR
0000	00E0	SYNC ERROR
0000	00FF	NO TEST SELECTED
0000	0008	NO CP SELECTED MASTER
0000	0007	NO RESPONSE FROM CDI/PCDC
0001	0001	NOTA ON MIU STATUS WRITE
0001	0002	NOT USED
0001	0003	NOTA ON MEMORY INITIALIZATION - ALL 0'S
0001	00EE	INTERRUPT (INTR1 OR 2) RECEIVED
0002	0009	NO MACRO INSTRUCTION DECODE
0002	0005	MICRO VECTOR ERROR - INCORRECT DECODE

Figure 38. Valid Error Displays for Failure of Normal Trace Steup for DCDTST.

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TYPE 2B PROCESSOR COMPLEX
SYSTEM MONITOR
STATIC AND DYNAMIC
INSTALLATION TEST PROCEDURES

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1. GENERAL

1.01 This section provides the static and dynamic installation test procedures for the System Monitor of the Type 2B Processor Complex.

2. FUNCTIONAL DESCRIPTION

2.01 The system monitor provides a means of monitoring software activity and certain internal central processor functions of the Central Processor Complex (CPC) in the common control system (Figures 1 through 3).

2.02 The two primary functions of the system monitor are to trace instruction flow within a Central Processor Unit (CPU) by monitoring addresses of instructions being executed and to trace data flow for a selected system bus function by monitoring the system command bus and system response bus along with status information from an active CPU.

2.03 Secondary functions of the system monitor include monitoring changes to the General Registers (GR0 through GR7) during instruction traces and performing a self-test upon command from the system monitor operator.

2.04 Modules may be installed in the system monitor to provide an X-ray test set subsystem. Printed wiring card slots are provided for up to 4K (where K = 1,024) by 48 bits of X-ray Read-Only Memory Simulator (ROMSIM), X-ray control card, and power supply. The system monitor control program contains the necessary software driver for loading the ROMSIM with microdiagnostics from a magnetic data cartridge to exercise a CPU.

2.05 The primary function of the X-ray test set subsystem is to provide a means for executing microdiagnostics by using a CPU within the common control system during system startup. A set of microdiagnostics can be used to establish confidence in the CPU, the memory system, the system buses, and certain Input/Output (I/O) devices to allow macrolevel software to be loaded through the system magnetic tape facility.

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2.06 The system monitor can be installed, operational software loaded, and self-tests performed without connection to the Type 2B Processor Complex. The trace buffer self-test requires connection to the system clocks.

2.07 All communication between the user and the system monitor is performed via a keyboard terminal, such as the Model 33 and Model 35 TTY. Model 300 and Model 1200 TERMINET® terminals, or comparable. The terminal can be either co-located with the system monitor or remotely located. Access to the system monitor from a remote site will be via standard voice grade dial-up or dedicated telephone lines.

2.08 Both the system monitor operational programs and the X-ray programs are loaded into the system monitor memory from 3M Company magnetic tape cartridges.

2.09 The system monitor is normally equipped with 1K by 48-bit Random Access Memory (RAM) on a ROMSIM card which is used to simulate the central processor unit Control Read-Only Memory (CROM) for X-ray testing.

3. PREREQUISITES

Documentation

3.01 The following documentation is required for performing the test procedures in this section:

(a) EL-15617 System Monitor - Circuit Design.

(b) 47-B-1018-0049 System Monitor - Engineering Prints.

(c) EXD-B-0005 System Monitor - Description and User's Guide.

® Registered trademark of General Electric Company.

Test Equipment

3.02 The following test equipment is required for performing the test procedures in this section:

(a) Oscilloscope, Tektronix 475 or equivalent.

(b) Volt-Ohmmeter (VOM).

(c) Backplane jumpers (daisy chain).

Procedures and Associated Illustrations

3.03 The following procedures are categorized into the different modes that the system monitor can be configured; these configurations should be performed sequentially for system start-up and may be individually performed as necessary:

(a) Initial bring-up.

(b) Memory loading.

(c) System monitor - Type 2B Processor Complex monitor cabling.

(d) Self-test.

(e) System monitor - Type 2B Processor Complex X-ray cabling.

(f) System monitor - Type 2B Processor Complex on-line cabling.

3.04 The procedures and information necessary for the Type 2B Processor Complex X-ray functions are included in the Type 2B Processor Complex X-ray installation test procedures.

3.05 All information relating to the correct operator's usage of the system monitor and X-ray functions are included in the Type 2B Processor Complex - System Monitor Description and User's Guide.

4. TEST OBJECTIVE

4.01 The objective of the test procedures in this section is to provide the information necessary for installation and self-testing of the system monitor prior to its use for Type 2B Processor Complex X-ray and/or system software monitoring.

5. TEST PROCEDURES

5.01 The following paragraphs cover the various installation test procedures for the system monitor.

Initial Bring-Up

5.02 Perform the initial bring-up procedure in accordance with Table 1. Also see Table 2 and Figure 4.

5.03 Keyboard Terminal Interface. All communications between the user and the system monitor are performed via a keyboard terminal. A serial device controller circuit provides the interface between the microprocessor and the terminal. A panel-mounted wafer switch (interface type) allows selection of Electronic Industries Association (EIA) RS232C, 12-volt/20 mA loop, 50-volt/20 mA loop or modem card (for use with a remotely located terminal). Also provided is a second panel-mounted wafer switch (baud rate) allowing selection of terminal operating speeds of 100, 300, or 1,200 characters per second (cps).

5.04 Remote Terminal Implementation. The system monitor can be controlled by a remotely located terminal. The optional modem card (FB-15092), available with the system monitor, is a 300-baud, FSK, answer-only type, that is operationally compatible with the Bell 103F Type Data Set. The modem can be connected to a standard voice-grade dial-up telephone line via a commercially available acoustic coupler and standard telephone subset, or to a dedicated telephone line. The implementation procedure is as follows:

(a) Connect the output of the modem screw-type terminals, to a telephone line by either the direct method or via the acoustic coupler.

(b) Set the interface-type switch to MODEM.

(c) Set the baud rate switch to the desired terminal speed (10 or 30 cps).

NOTE: The interface-type switch only affects information received by the serial device controller. Information transmitted by the serial device controller is sent on all ports, EIA, 12-volt/20-mA, 50-volt/20-mA, and modem, simultaneously.

Operational Program Memory Loading

5.05 Perform the initial program load test for operational program memory loading in accordance with Table 3. Also see Figure 5.

5.06 Operational Memory Test. The Operational Memory (OP MEM) test is resident in the 8080 microprocessor Read-Only Memory (ROM) and will perform a basic sanity test on the 16K by 8-bit operational Random-Access Memory (RAM) automatically. This test is initiated as a function of the memory loader RESET pushbutton and LOAD ENABLE switch, located on file C of the system monitor backplane, before the operational ROM bootstrap loader is executed.

5.07 Successful execution of the OP MEM test results in automatic loading of the operational RAM from the magnetic tape cartridge.

5.08 Unsuccessful execution of the OP MEM test results in terminal output of the following data:

(a) OP MEM TEST FAILURE 0

(b) OP MEM TEST FAILURE 1

5.09 For isolation of memory addresses and associated card location, the following apply:

OP MEM TEST FAILURE	MEMORY ADDR	CARD	LOCATION
0	C000-DFFF	FB-20723	B18
1	E000-FFFF	FB-20723	B16

5.10 Manual Routine Hardware. If a problem is detected during normal operation or during execution of the test phase, a knowledgeable maintenance person can manually routine the hardware. This is accomplished by inserting the test

panel interface card (FB-20712), which has cable connections to the manual routiner panel (HS 851111). The combination of the test panel interface circuit and manual routiner panel allows the maintenance person access to the microprocessor external bus system and associated circuitry.

5.11 The manual routiner consists of a briefcase-mounted panel with various readouts, switches, and indicators. The test panel interface circuit is a Standard Hardware Electronic Systems (SHES) 13-inch card that contains the necessary electronics to interface the panel with the microprocessor external bus system. The test panel interface circuit is located in slot C14.

5.12 The panel displays the following microprocessor external buses: MA00 through MA15, MD00 through MD07, and MD10 through MD17. Also, it can perform Direct Memory Access (DMA) reads and writes from/to memory and controls the state of the microprocessor by use of the ready and Hold Request (HOREQ) levels. The following is a complete list of features provided with the panel:

(a) Run - CPU executing instructions.

(b) Halt - CPU bus system placed in high-impedance state.

(c) Step - CPU executes one instruction at a time.

(d) Reset - microprocessor system reset.

(e) Write memory - DMA write into memory. The CPU must be in the halt state.

(f) Read memory - DMA read from memory. The CPU must be in the halt state.

(g) Rewind - causes the cartridge tape reader to rewind tape.

(h) Panel interrupt - not used.

(i) Memory watch - update data display upon address match.

(j) Address match - when implemented, stops the microprocessor when the address bus data equals the panel address display.

(k) Advance one - increments the panel memory address counter by one.

(l) Panel reset - resets the internal panel logic.

(m) Display reset - resets the address and data displays.

(n) Load data - allows loading of data into the data display.

(o) Load address - allows loading of data into the address display.

(p) BOT - Beginning Of Tape (BOT) - BOT (cartridge) indicator.

(q) EOT - End Of Tape (EOT) - EOT (cartridge) indicator.

NOTE: Power for the manual routiner panel and test panel interface circuit is obtained from the system monitor power distribution.

5.13 Terminal Requests/Commands/Responses. The following describe the commands entered on the system keyboard terminal that enable the user to communicate with the system monitor:

(a) Basic monitor commands. The system monitor control program recognizes two types of keyboard-entered data: monitor commands and prompter responses. Monitor commands are initiated by the user to alert or control the main scan portion of the system monitor control program. Prompter responses are data entered by the user in response to prompter questions.

(b) Control characters. The following characters, when entered on the keyboard terminal, are recognized by the system monitor program as control characters:

(1) CTL-X (CAN) - aborts operation and return to monitor program.

(2) CTL-B (STX) - indicates beginning of monitor command.

(3) CTL-C (ETX) - indicates end of monitor command or response to prompter.

(4) CTL-Z (SUB) - used only after a load command.

(5) $ (dollar sign)- terminal-entered character deletion.

(c) Monitor command input format. When the monitor program recognizes a CTL-B entered on the keyboard terminal, an I* is printed, beginning at column 1. Then, the user enters the monitor command and the CTL-C (ETX) indicates the end of the command, and the monitor program begins. Example:

<STX>

I* <COMMAND><ETX>

where <> specifies user's input

(d) Prompter response input format. A prompter response is required whenever a prompter question is generated by the monitor program. A prompter response can consist of either hexadecimal data or one of the possible choices indicated in the prompter question. Example:

'Prompter Question =' <Prompter Response><ETX>

where <> specifies user's input

(e) Error condition. The control character $ (dollar sign) is used for character deletion. Each $ entered via the terminal deletes one previously entered character. Example:

4 START(ADDR,EXT,IMMED)= <IMMA$ED><ETX>

where <> specifies user's input

(f) Line deletion. The process for deleting a complete line of data is to enter a CTL-B (STX). All data entered on the line is deleted. Example:

4 START(ADDR,EXT,IMMED)=<IMMED><STX><ADDR><ETX>5 ETC.

where <> specifies user's input

5.14 Operational Memory Reload. If a fault is suspected with the operational program, the user may elect to perform a memory reload. This feature is provided by the load monitor command which, when entered, indicates to the program to perform a memory reload from the magnetic tape cartridge. This command assumes certain portions of the operational program are intact (sane)

when the command is issued and allows a user at a remote location to perform a program reload via the keyboard terminal. Of course, the magnetic tape cartridge must be inserted correctly into the magnetic tape drive assembly.

5.15 All hardware initialization and self-tests are performed as if this was a bootstrap (initial) program load. Example:

<ETX>

I*<LOAD><SUB><ETX>

LOAD OK

Monitor Cabling/Configuration

5.16 The system monitor, when used as a macrosoftware monitor, does not require hardware connections (Tables 4 and 5) to internal CP points and also does not require a specific CP configuration for operation. (Refer to Figure 1 for the system configuration.) However, the monitor configuration is required for X-ray configuration regardless of the CP configuration. Also, see Figure 6.

Self-Tests

5.17 Monitor Self-Test (BTEST). After an operational program load is successfully completed, the hardware initialization will be rerun, plus, the BTEST feature will be performed to verify the data path and trace buffer memory fabric of the system monitor (refer to Figure 7).

5.18 The test consists of loading the trace buffer with various static and dynamic test patterns through the trace data multiplexer. This method verifies the major data paths used in capturing trace data and associated control paths.

5.19 The test is divided into five separate phases with one phase being associated with each of the buffer array cards (FB-15671, slots B24, B26, B28, B30, and B32). The following will be printed as each of the five phases is completed. Example:

BTEST: 01

ATP

.

.

.

.

BTEST: 05

ATP

5.20 The BTEST N command test may also be executed by a terminal-initiated command request any time after a successful operational program load. The value of N can range from 0 to 5 and indicates the following:

0 = Execute all five phases

N Phase	Microprocessor Address Range	Buffer Array Card Location
1	2000-2FFF	B24
2	4000-4FFF	B26
3	6000-6FFF	B28
4	8000-8FFF	B30
5	A000-AFFF	B32

5.21 For BTEST errors, if an error is detected during the test, the following data is printed for each faulty trace location:

(a) The address of the faulty trace buffer location (ADDR).

(b) The correct data pattern sent to the trace buffer location (CP).

(c) The failing data pattern read from the trace buffer location (FP).

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5.22 The user can interrupt the printout of the faulty trace buffer locations by entering an STX command. Example:

<ETX>

I*<BTEST 0><ETX>

BTEST:01

ATP

BTEST:02

ADDR	CP	FP
4000	55	54
4001	55	54
4002	55	54

<STX>

BTEST:03

ATP

BTEST:04

ATP

BTEST:05

ATP

5.23 X-ray (ROMSIM) Self-Test. The first time the X-ray control section is entered, an X-ray self-test is executed upon any ROMSIM installed cards.

5.24 The test consists of loading the ROMSIM with various patterns and reading them back through the 8080 microprocessor interface. The program will test all ROMSIM installed in the system, up to a maximum of 4K as follows:

(a) The X-ray self-test is divided into four phases, with each phase being associated with a 1K page of ROMSIM (FB-15673, slots A11, A13, and A15 for pages 1 and 2; A10, 12, 14 for pages 3 and 4):

(1) X-ray control entered for the first time. Example:

READY (Y, N, E, X, A) = <X><ETX>

XRAY

X-RAY MAX SIZE = 1K

XTEST:01

ATP

(2) X-ray control previously entered. Example:

<STX>

I*<XRAY><ETX>

XRAY

X-RAY (S,L,E,EM,I,T,P,C) = <T><ETX>

X-TEST (0,1,2,3,4) = <0><ETX>

X-RAY MAX SIZE = 1K

XTEST:01

ATP

NOTE: A page selection of zero (0) indicates that all available ROMSIM will be tested. If a specific page is selected, only that page will be tested.

TEST PHASE (PAGE)	MICROPROCESSOR ADDRESS RANGE	ROMSIM CARD LOCATION
1 and 2	0800-0FFF	A11
	1000-17FF	A13
	1800-1FFF	A15
3 and 4	0800-0FFF	A10
	1000-17FF	A12
	1800-1FFF	A14

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(b) X-ray test errors. If an error is detected during the test, the following data is printed for each faulty ROMSIM location:

(1) The address of the faulty ROMSIM location (ADDR).

(2) The correct data pattern sent to the ROMSIM location (CP).

(3) The failing data pattern read from the ROMSIM location (FP).

The user can interrupt the printout of the faulty ROMSIM locations by entering an STX command. Example:

```
X-RAY (S,L,E,EM,I,T,P,C) =<T><ETX>
X-TEST (0,1,2,3,4) =<0><ETX>
X-RAY MAX SIZE = 2K
XTEST:01
ADDR      CP   FP
1000      AA   2A
1001      AA   2A
1002      AA   2A
1000      FF   7F
1001      FF   7F
1002      FF   7F
<STX>
XTEST:02
ATP
```

X-ray Cabling/Configuration

5.25 Only one central processor can be X-ray tested by the system monitor at any one time; therefore, there are three different configurations, depending upon which central processor is to be tested. These configurations can only be used on an off-line system and are intended for initial system startup X-rays only. (See Tables 6 and 7.)

5.26 The X-ray programs depend upon the tracing functions of the system monitor. It is necessary for the system monitor and central processors to be configured in the monitor configuration. (Refer to paragraphs 5.17 through 5.24 and Figures 8 through 14.) However, the X-ray configuration is not required for the monitor mode.

5.27 The X-ray configuration does require connections to internal central processor functional points. This is provided by connection of the system monitor X-ray buffer card (FB-15675) to the central processor foreplane cable between the SEQ2 (FB-15650) and SEQ1 (FB-15649) cards. There also are chip clip connections from the X-ray buffer to the central processor System Monitor Interface (SMI) (FB-15655) and BCTL1 (FB-15651) cards.

5.28 The X-ray function also requires backplane straps on the Central Processor Complex Frame (CPCF), which forces the selected X-ray central processor to be the master central processor.

5.29 Because of critical central processor timing functions, cables between the X-ray ROMSIM and the X-ray buffer must not be longer than five feet.

On-Line Monitor Cabling/Configuration

5.30 It may be necessary to connect the system monitor to an on-line processor complex to monitor system software problems (Table 8). This requires that only the system monitor CPCF configuration be used.

5.31 With an on-line system, certain precautions must be taken to preclude the occurrence of a system outage. The procedure given in this section must be followed exactly, with no deviations. This procedure assumes that the central processors are in a full triplex configuration and will systematically routine, take off-line, power down, cable, power up, routine, and place on-line each processor in turn, beginning with CP2 through CP0.

00213

5.32 If noncritical problems exist in any central processors before the system monitor is connected, it is left to the operator's discretion whether to operate in this condition or correct the problems.

00214

Table 1. Initial Bring-Up Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Insert all power cards into the system monitor, disconnect all other cards, and set the main circuit breaker to OFF.	
2	Apply -50 Vdc via the receptacle (lower left panel).	
3	Install main fuse F1 (15 amperes), alarm fuse F2 (3 amperes) and F3 (amperes), and set the switch main circuit breaker to ON.	The Electronic Voltage Monitor (EVM) card FB-15277), file C, position 7, lamps (5-10), and the Power Control and Supervision Detect (PCSD) (FB-15228), file C, position 10, PWR OFF and OOS lamps light.
4	Depress the PWR REQ pushbutton on the PCSD (FB-15228) file C, position 10.	The EVM (C7) lamps (5-10) and the PCSD (C10) PWR OFF lamps go dark. On card FB-15228 (C10), the PWR ON and OOS lamps light.
5	Depress the PCSD (C10) PWR REQ pushbutton.	The results correspond to those in step 3.
6	Verify that the magnetic cartridge reader interface (flat-shielded) cable is connected to the magnetic tape cartridge drive assembly. NOTE: Connector pin 1 (top and to the left of notch) to cable pin 1 (marked in red).	

00215

Table 1. Initial Bring-Up Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
7	Insert all cards into their appropriate positions. (Refer to Figure 3 and EC-47-B-1018-0049.) NOTE: Test panel interface FB-20712 C14 should not be inserted unless the manual routiner (HS 851111) is connected.	
8	Connect the flat ribbon cable (ID 1) to the J1 connectors of cards A22, A24, A25, A26, A27, and A28. NOTE: All foreplane cables are to be connected with pin 1 to the lower right.	
9	Connect the twisted ribbon cable (ID 2) to the J1 connectors of cards B34 and B36.	
10	Verify that the magnetic cartridge reader interface flat-shielded cable is connected to FB-20697 (C18-J1 cable ID 3).	

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Table 1. Initial Bring-Up Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
11	Connect the local or remote terminal interface to the appropriate cable terminations on FB-15621 (B14 cable ID 4). Select appropriate terminal characteristics on the switch panel located in the file C backplane of the system monitor. (Refer to paragraphs 5.03 and 5.04.)	
12	Depress the PCSD PWR REQ pushbuttons.	The results correspond to those in step 4.

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Table 2. Operational Program Memory Loading-Initial Program Load.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Insert the cartridge assembly of the system monitor operational load into the magnetic tape cartridge drive assembly (FD-5000-BR).	
2	Set the toggle switch one the backplane switch panel to the load enable (up) position. NOTE: If switches are mounted on the FB-20697 (C18) and FB-20725 (C19) cards, they should be in the down position.	
3	Depress the RESET push-button on the backplane switch panel.	If the cartridge is not inserted or seated properly, a CARTRIDGE IS OUT message is printed.
4	Release the RESET pushbutton.	The following occur: (a) A hardware initialization is automatically performed on the 8080 microprocessor control and interface circuits. (b) If a blank cartridge is inserted, the program will search the tape and give no response. (c) An operational memory test (OP MEM TEST) will automatically be performed (16K x 8-bit RAM) OP MEM TEST ATP SUCCESSFUL. The cartridge tape rewinds to the Beginning of Tape (BOT) and then starts in a forward motion. (d) OP MEM TEST FAILURE 0 to 1. (Refer to paragraphs 5.06 through 5.09.) (e) Successful operational program load. LOAD OK The tape motion continues until the End of Tape (EOT) and then stops.

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Table 2. Operational Program Memory Loading - Initial Program Load (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
		(f) If there is a failure on operational program load, repeat steps 1 through 3 and/or connect the manual routiner, and attempt to isolate/resolve the problem. (Refer to paragraphs 5.10 through 5.12.)

NOTE: Immediately following a successful operational program load, an automatic test will be performed on the trace buffer data multiplexer circuitry and trace buffer memory fabric. (Refer to paragraph 5.16.)

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Table 3. Initial System Monitor Loading.

CABLE ID	POS	CONN	FB	CARD DESC		POS	CONN	FB	CARD DESC	CABLE TYPE
1	A22	J1	15667	TRACE SETUP & CONTROL	——	A24	J1	15666	TRACE DATA MUX	FLAT RIBBON
					——	A25				
					——	A26				
					——	A27				
					——	A28				
2	B34	J1	15665	BUS RCVR/ PIPE	——	B36	J1	15665	BUS RCVR/ PIPE	TWISTED RIBBON
3	C18	J1	20697	MAG CART READER INTF	——	C22-36		FD 5000-BR	3M MAG TAPE DRIVE	FLAT SHIELDED
4	B14	TAB A	15621	SERIAL DEVICE CONTR	——	TTY/ TERMINET	EC-11969 ASSY A		12v/20MA	DATA CABLE
OR		TAB C			——		EC-11969 -B		E1A	
OR		TAB D			——		EC-11969 ASSY A		50V/20MA	

00220

Table 4. Monitor Cabling Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Depress the PCSD (C10) PWR REQ pushbutton.	The EVM (C7) lamps (5-10) and the PCSD PWR OFF and OOS lamps light.
2	Depress the PCSD PWR REQ pushbuttons on the Central Processor Memory C FRAME (CPCF) (CP0-F10, CP1-G5, CP2-H5) for each CP.	The EVM (D13, 17, 21) lamps and the PCSD PWR OFF and OOS lamps light.
3	Connect the CPCF cables (5-17) as depicted in table 3 and figures 9 and 10.	
4	Depress the PCSD PWR REQ pushbuttons on the CPCF (CP0-F10, CP1-G5, CP2-H5) for each CP.	The EVM (D13, 17, 21) lamps and the PCSD PWR OFF and OOS lamps go dark. The PCSD PWR ON lamps light.
5	Depress the PCSD PWR REQ pushbutton.	The EVM (C7) lamps (5-10) and the PCSD PWR OFF and OOS lamps go dark. The PCSD PWR ON lamp lights.

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Table 5. Monitor Cabling.

CABLE ID	FRAME	POS	CONN	FB	CARD	TO	FRAME	POS	CONN	FB	CARD	CABLE TYPE
5	SM	A30	J1	15665	BUS RCVR/ PIPE	——	CPCF	TA9	J1	15654	MATCHER LEFT CMD BUS 0	TWISTED RIBBON
6		A30	J2			——		TA9	J2			
7		A32	J1			——		A27	J1	15658	MATCHER RIGHT CMD BUS 1	
8		A32	J2			——		A27	J2			
9		A34	J1			——		F36	J1		MATCHER A RSP BUS 0	
10		A34	J2			——		F36	J2			
11		A36	J1			——		G10	J1		MATCHER B RSP BUS 1	
12		A36	J2			——		G10	J2			
13		BACK PLANE B36	J1	15656	CLOCK TERM	——		B17	J1A	15660	MASTER CLOCK	COAXIAL 20'
14			J2			——		C17	J1B	15661	SLAVE CLOCK	COAXIAL 20'
15	CPCF	B17	J1B	15660	MASTER CLOCK	——		C17	J1A			COAXIAL 2'
16	SM	B36	J2	15668	BUS RCVR 1	——		H30	J2	15655	SM1 CP2	FLAT SHIELDED
						——		G30	J2		SM1 CP1	
						——		F32	J2		SM1 CP0	
17	SM	B34	J2	15672	BUS RCVR 2	——		H30	J1		SM1 CP2	FLAT SHIELDED
						——		G30	J1		SM1 CP1	
						——		F32	J1		SM1 CP0	

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Table 6. X-Ray Cabling Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Depress the PCSD (C10) PWR REQ pushbutton.	The EVM (C7) lamps (5-10) and the PCSD lamps PWR OFF and OOS lamps light.
2	Depress the PCSD PWR REQ pushbuttons (CP0-F10, CP1-G5, CP2-H5) on the CPCF for the selected or all CP(s).	The EVM (D13, 17, 21) lamps and the PCSD PWR OFF and OOS lamps light.
3	Connect the CPCF cables (18-25) for the selected CP as depicted in table 7 and figures 11 through 14. NOTE: Intercard cables (ID 23 and 24) are to be connected with pin 1 on the upper right.	
4	Depress the PCSD PWR REQ pushbuttons on the CPCF for all CP(s).	The EVM lamps and the PCSD PWR OFF and OOS lamps go dark. The PCSD PWR ON lamps light.
5	Depress the PCSD PWR REQ pushbutton.	The EVM lamps (5-10) and PCSD PWR OFF and OOS lamps go dark. The PCSD PWR ON lamp lights.

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Table 7. X-Ray Cabling.

	CABLE ID	FRAME	POS	CONN	FB	CARD DESC		FRAME	POS	CONN	FB	CARD DESC	CABLE TYPE
CP0	18	SM	A11	J2	15673	X-RAY ROMSIM	——	CPCF	FORE-PLANE F15/16	J5	15675	X-RAY BUFFER	TWISTED RIBBON
	19		A13				——			J4			
	20		A15				——			J3			
	21		A17		15674	X-RAY CONTROL	——			J6			
	22		BACK-PLANE A	MOLEX P1		POWER CONN	——			MOLEX P1			POWER CABLE
	23	CPCF	F32	CHIP M92	15655	SM1	——			CHIP U9			TWISTED RIBBON
	24		F22	CHIP N84	15651	BCTL1	——			CHIP J80			TWISTED PAIR
*	25		BACK-PLANE	GRND			——		BACK-PLANE F16	PIN 32	15649	SEQ 1	JUMPER STRAP
CP1	18	SM	A11	J2	15673	X-RAY ROMSIM	——	CPCF	FORE-PLANE G13/14	J5	15675	X-RAY BUFFER	TWISTED PAIR
	19		A13				——			J4			
	20		A15				——			J3			

00224

Table 7. X-Ray Cabling (Continued).

CABLE ID	FRAME	POS	CONN	FB	CARD DESC		FRAME	POS	CONN	FB	CARD DESC	CABLE TYPE
21	SM	A17	J2	15674	X-RAY CONTROL	——	CPCF	FORE-PLANE G13/14	J6	15675	X-RAY BUFFER	TWISTED PAIR
22	↓	BACK-PLANE A	MOLEX P1		POWER CONN	——	↓	↓	P1	↓	↓	POWER CABLE
23	CPCF	G30	CHIP M92	15655	SM1	——	↓	↓	CHIP U9	↓	↓	TWISTED RIBBON
24	↓	G20	CHIP N84	15651	BCTL1	——	↓	↓	CHIP J80	↓	↓	TWISTED PAIR
25	↓	BACK-PLANE	GRND			——	↓	BACK-PLANE G14	PIN 32	15649	SEQ1	JUMPER STRAP
18	SM	A11	J2	15673	X-RAY ROMSIM	——	CPCF	FORE-PLANE H13/14	J5	15675	X-RAY BUFFER	TWISTED RIBBON
19	↓	A13	↓	↓	↓	——	↓	↓	J4	↓	↓	↓
20	↓	A15	↓	↓	↓	——	↓	↓	J3	↓	↓	↓
21	↓	A17	↓	15674	X-RAY CONTROL	——	↓	↓	J6	↓	↓	↓
22	↓	BACK-PLANE A	MOLEX P1	↓	POWER CONN	——	↓	↓	P1	↓	↓	POWER CABLE
23	CPCF	H30	CHIP M92	15655	CM1	——	↓	↓	CHIP U9	↓	↓	TWISTED RIBBON

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*

CP2

00225

Table 7. X-Ray Cabling (Continued).

CABLE ID	FRAME	POS	CONN	FB	CARD DESC	TO	FRAME	POS	CONN	FB	CARD DESC	CABLE TYPE
24	CPCF	H20	CHIP N84	15651	BCTL1	——	CPCF	FORE-PLANE H13/14	CHIP J80	15675	X-RAY BUFFER	TWISTED PAIR
25	↓	BACK-PLANE	GRND			——	↓	BACK-PLANE H14	PIN 32	15649	SEQ 1	JUMPER STRAP

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Table 8. On-Line Monitor Cabling/Configuration Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Configure the System Monitor for initial bring-up (paragraphs 5.01 through 5.04).	Refer to paragraphs 5.01 through 5.04.
2	Perform the System Monitor initial program load (paragraphs 5.05 through 5.15).	Refer to paragraphs 5.05 through 5.15.
3	Perform the System Monitor cabling (paragraph 5.16), but only connect the system monitor side of the cables (leaving the CPCF side of the cables unconnected figure 9). Also omit step 5 of this procedure, leaving the system monitor powered down.	Refer to paragraph 5.16.
4	Routine CP2 with system diagnostics for an All-Tests-Passed (ATP) condition. This ensures that when the system monitor and CP are connected, and there are no faults introduced. Input ROUT CP2	The terminal outputs a message indicating ATP. NOTE: If a trouble number fault does exist and is not critical to system performance, the procedure may be continued. If a critical fault does exist, it is best to repair the fault before continuing, but the CP may also be taken out of service for this procedure.

00227

Table 8. On-Line Monitor Cabling/Configuration Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
5	Input PUT CP2 OOS	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP2 INS.ACT TO OOS.MM The PCDC CP2 OOS and PCSD (H5) OOS lamps light.
6	Power-down CP2 by depressing the PCSD (H5) PWR REQ pushbutton.	CP2 is powered-down. The EVM (D21) and PCSD PWR OFF lamps light.
7	Refer to Table 5 and Figure 10 to connect cables 5 through 15 and only the H30 J1 and J2 connections of cables 16 and 17.	
8	Power-up CP2 by depressing the PCSD (H5) PWR REQ pushbutton.	The EVM (D21) and PCSD PWR OFF lamps go dark.
9	Input PUT INS CP2	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP2 OOS.MM TO INS.ACT The PCDC CP2 OOS and PCSD (H5) OOS lamps go dark.
10	Input ROUT CP1	The terminal outputs a message indicating ATP.

00228

Table 8. On-Line Monitor Cabling/Configuration Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
11	Input PUT OOS CP1	The terminal outputs OK JOB:XXXX R@XXXX JOBL:XXXX STATUS CHANGE CP2 INS.ACT TO OOS.MM The PCSD (G5) OOS and PCDC CP1 OOS lamps light.
12	Power-down CP1 by depressing the PCSD (G5) PWR REQ pushbutton.	CP1 is powered-down. The EVM (D17) and PCSD (G5) PWR OFF lamps light.
13	Refer to Table 5 and Figure 10 to connect only the G30 J1 and J2 connectors of cables 16 and 17.	
14	Input PUT ACT CP1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP1 OOS.MM TO INS.ACT The PCDC CP1 OOS and PCSD (G5) OOS lamps go dark.
15	Input ROUT CP0	The terminal outputs a message indicating ATP.
16	Input PUT OOS CP0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP0 INS.ACT TO OOS.MM

00229

Table 8. On-Line Monitor Cabling/Configuration Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
		The PCSD (F10) OOS and PCDC CP0 OOS lamps light.
17	Power-down CP0 by depressing the PCSD (F10) PWR REQ pushbutton.	CP0 is powered-down The EVM (D13) lamps and PCSD (F10) PWR OFF lamps light.
18	Refer to Table 5 and Figure 10 to connect the remaining F32 J1 and J2 connectors of cables 16 and 17.	
19	Input PUT ACT CP0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP0 OOS.MM TO INS.ACT The PCDC CP0 OOS and PCSD (F10) OOS lamps go dark.
20	At this point, all CPCF system monitor cables should be connected at both ends and the triplex CP's should all be on-line and processing without (or with known noncritical) faults.	
21	Disconnect the ROMSIM cards (FB-15673) A11, 13, 15.	

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Table 8. On-Line Monitor Cabling/Configuration Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
22	Using backplane straps, jumper the following pins on the system monitor backplane: POS A13: PIN 42-97, 44-43, 46-45, 47-48, 95-93, 96-94 POS A15: PIN 42-97, 44-43, 46-45, 47-48, 95-93, 96-94	
23	Power up the system monitor by depressing the PCSD PWR REQ pushbutton.	The EVM (C7) lamps (5-10) and PCSD PWR OFF and OOS lamps go dark. The PCSD PWR ON lamp lights.
24	Perform the tests in paragraphs 5.05 through 5.15 and 5.17 through 5.22.	Refer to paragraphs 5.05 through 5.15 and 5.17 through 5.22.

NOTE: The system monitor/CPCF configuration should now be capable of performing software tracing functions with no adverse effect upon the system. Refer to the System Monitor Description and User's Guide (EXD-B-0005) for operating instructions.

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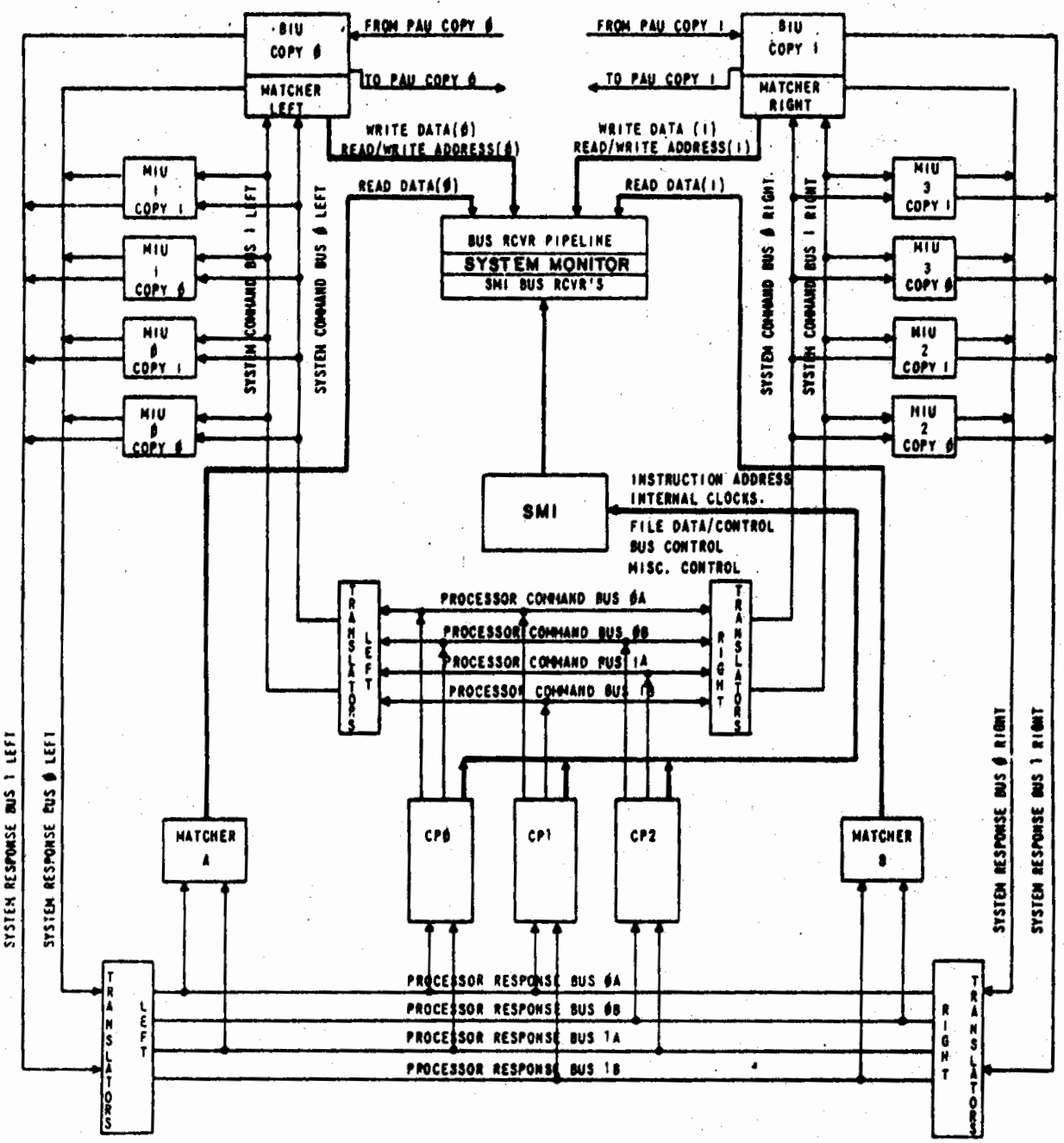


Figure 1. System Monitor CPU Monitor Configuration.

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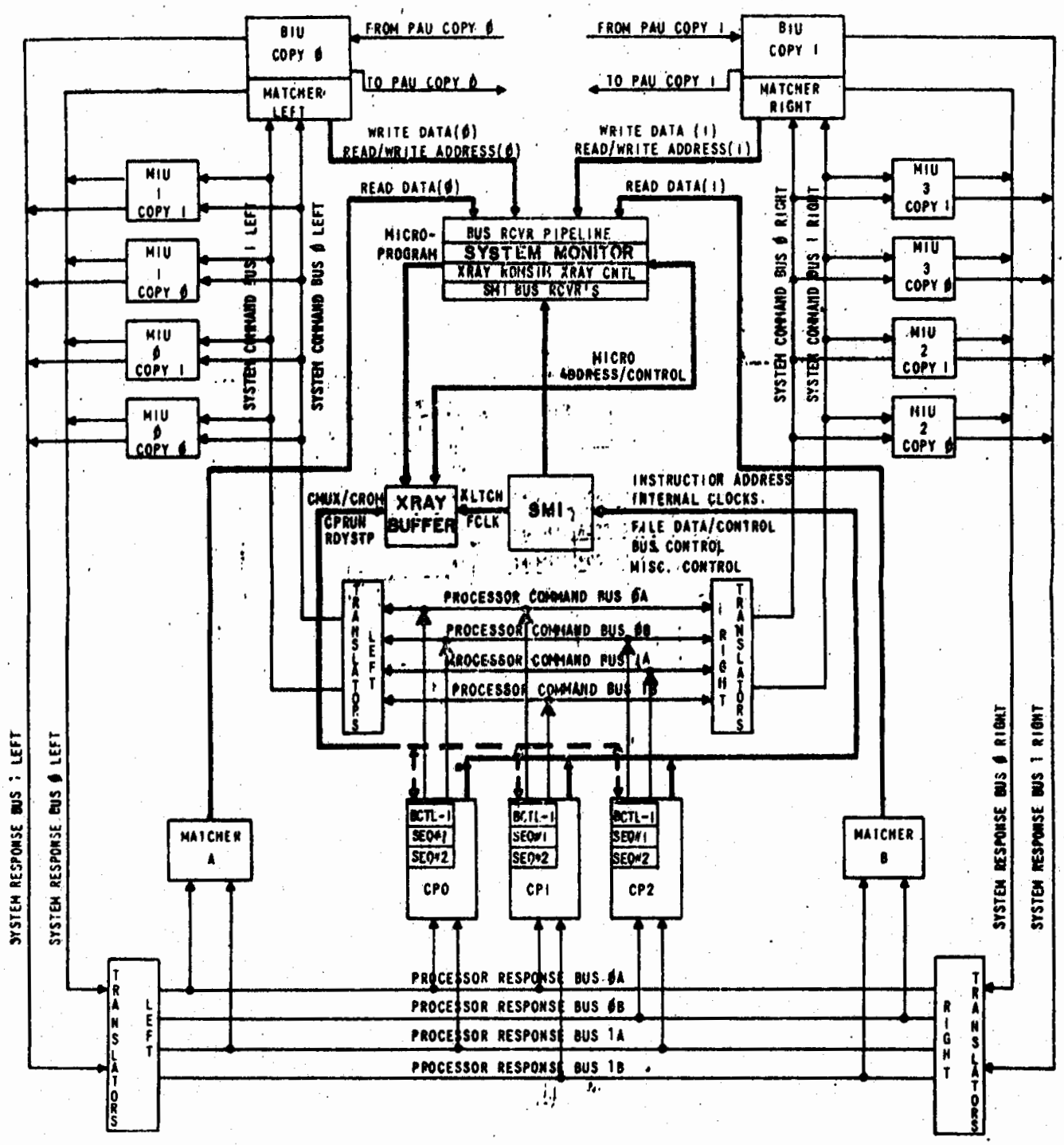


Figure 2. System Monitor CPU X-ray Configuration.

FILE C CIRCUIT BREAKER ASSY	FILE B	FILE A	
FB-15438 ±12V CV/CT	FB-15002 +5V CV/CT	FB-10002 +5V CV/CT	1
			2
			3
FB-10745 ±18V CV/CT	FB-15003 +5V CV	FB-15003 +5V CV	4
			5
			6
FB-15227 EVM	FB-15003 +5V CV	FB-15003 +5V CV	7
			8
			9
FB-15228 PCSD	FB-15003 +5V CV	FB-15673 OPTIONAL X-RAY ROMSIM	10
		FB-15673 X-RAY ROMSIM	11
		FB-15673 OPTIONAL X-RAY ROMSIM	12
		FB-15673 X-RAY ROMSIM	13
FB-20712 TST PNL INTF	FB-15621 SERIAL DEV CONT	FB-15673 OPTIONAL X-RAY ROMSIM	14
		FB-15673 X-RAY ROMSIM	15
FB-15092 MODEM	FB-20723 8K X8 RAM		16
		FB-15674 X-RAY CONTROL	17
FB-20697 CART READ INTF	FB-20723 8K X8 RAM	FB-15008 DATA MATCHER	18
FB-20725 CART WRT INTF			19
3M CARTRIDGE TAPE DRIVE FD-5000-BR	FB-15817 8080 UP	FB-15007 ADDR MATCHER	20
			21
	FB-15664 BUFF MEM CONT	FB-15667 TRACE SETUP&CNTL	22
			23
	FB-15671 BUFF ARRAY	FB-15666 TRACE DATA MUX	24
		FB-15666 TRACE DATA MUX	25
	FB-15671 BUFF ARRAY	FB-15666 TRACE DATA MUX	26
		FB-15666 TRACE DATA MUX	27
	FB-15671 BUFF ARRAY	FB-15666 TRACE DATA MUX	28
		FB-15007 ADDR MATCHER	29
	FB-15671 BUFF ARRAY	FB-15665 BUS RCVR/PIPELINE	30
			31
	FB-15671 BUFF ARRAY	FB-15665 BUS RCVR/PIPELINE	32
			33
	FB-15672 SMI BUS RCVR #2	FB-15665 BUS RCVR/PIPELINE	34
			35
	FB-15668 SMI BUS RCVR #1	FB-15665 BUS RCVR/PIPELINE	36

Figure 3. System Monitor Frame Image - Front View.

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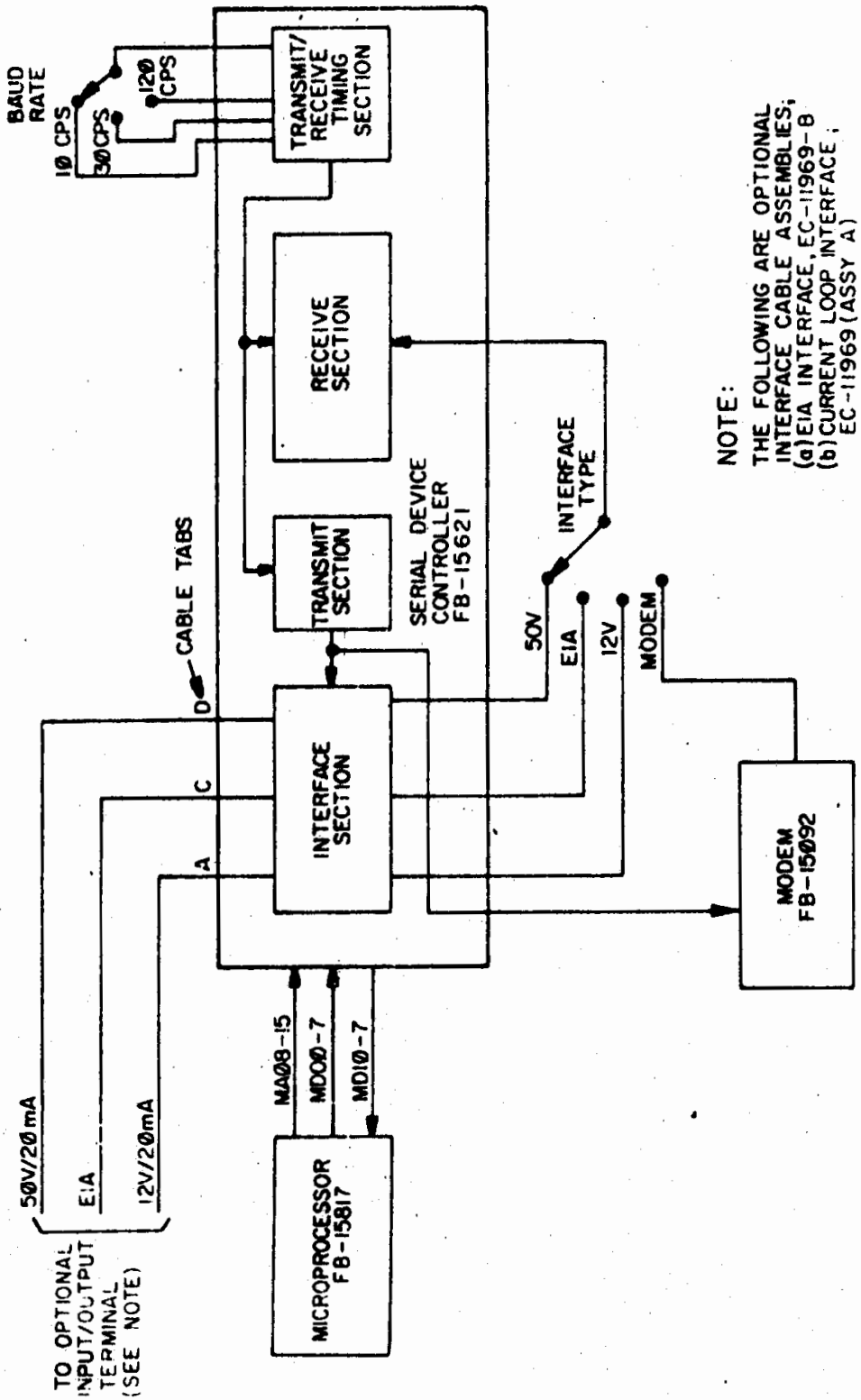


Figure 4. I/O Terminal Interface and Band Rate Selection.

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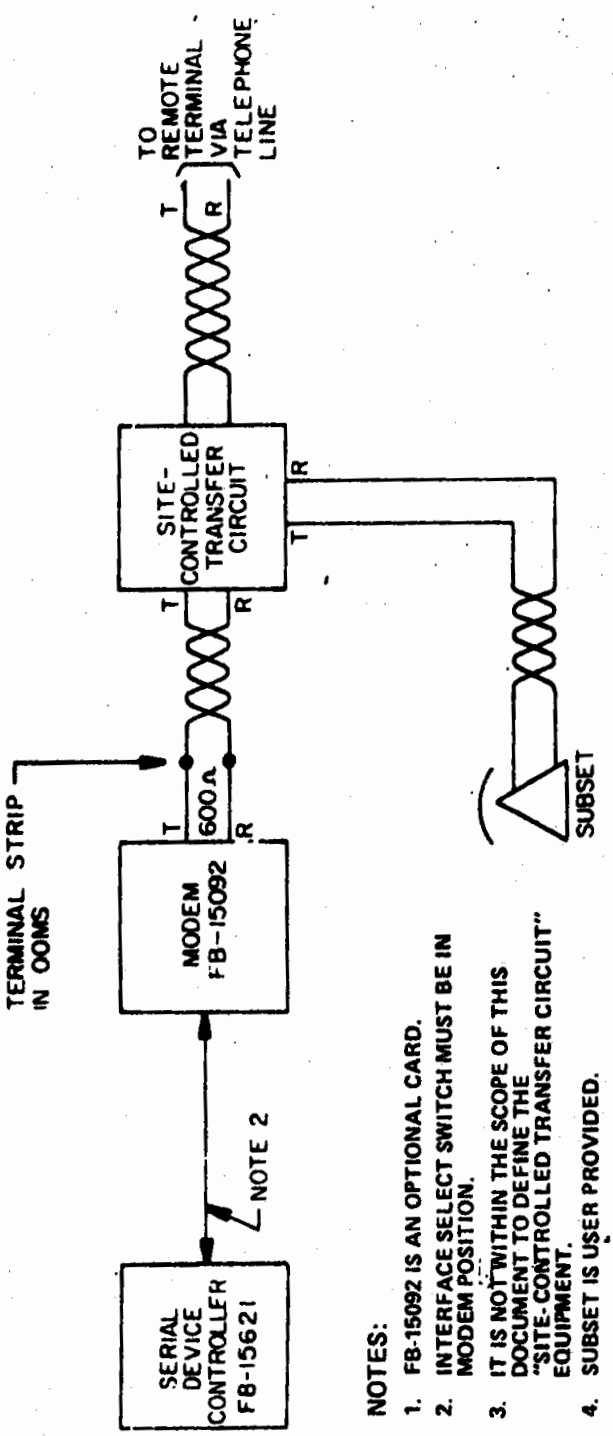


Figure 5. Configuration for Remote Terminal Implementation (Direct Method).

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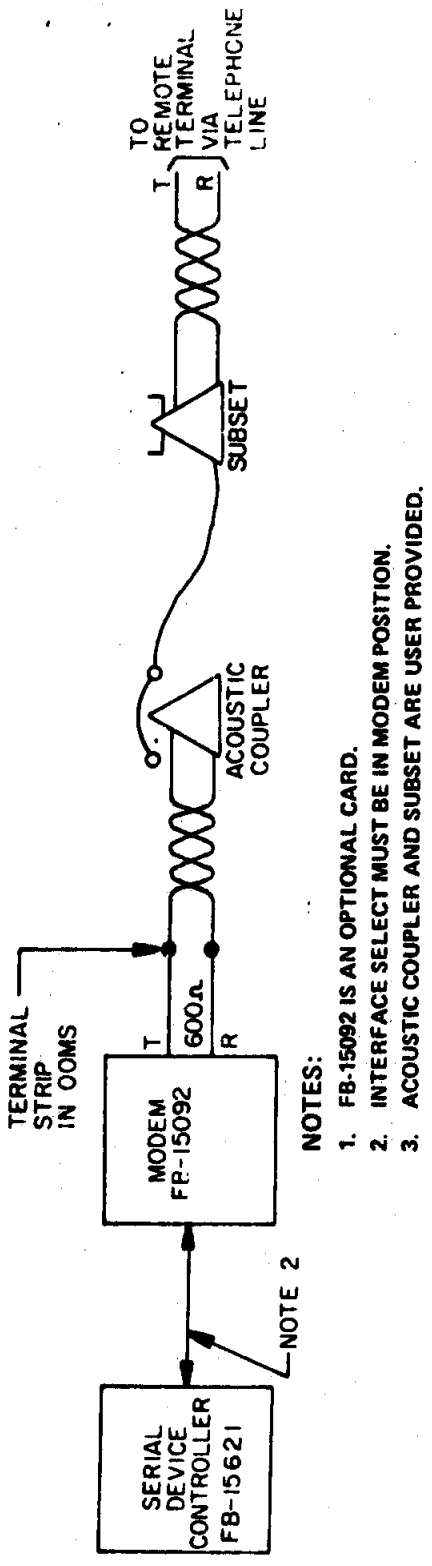


Figure 6. Configuration for Remote Terminal Implementation (Acoustic Coupler Method).

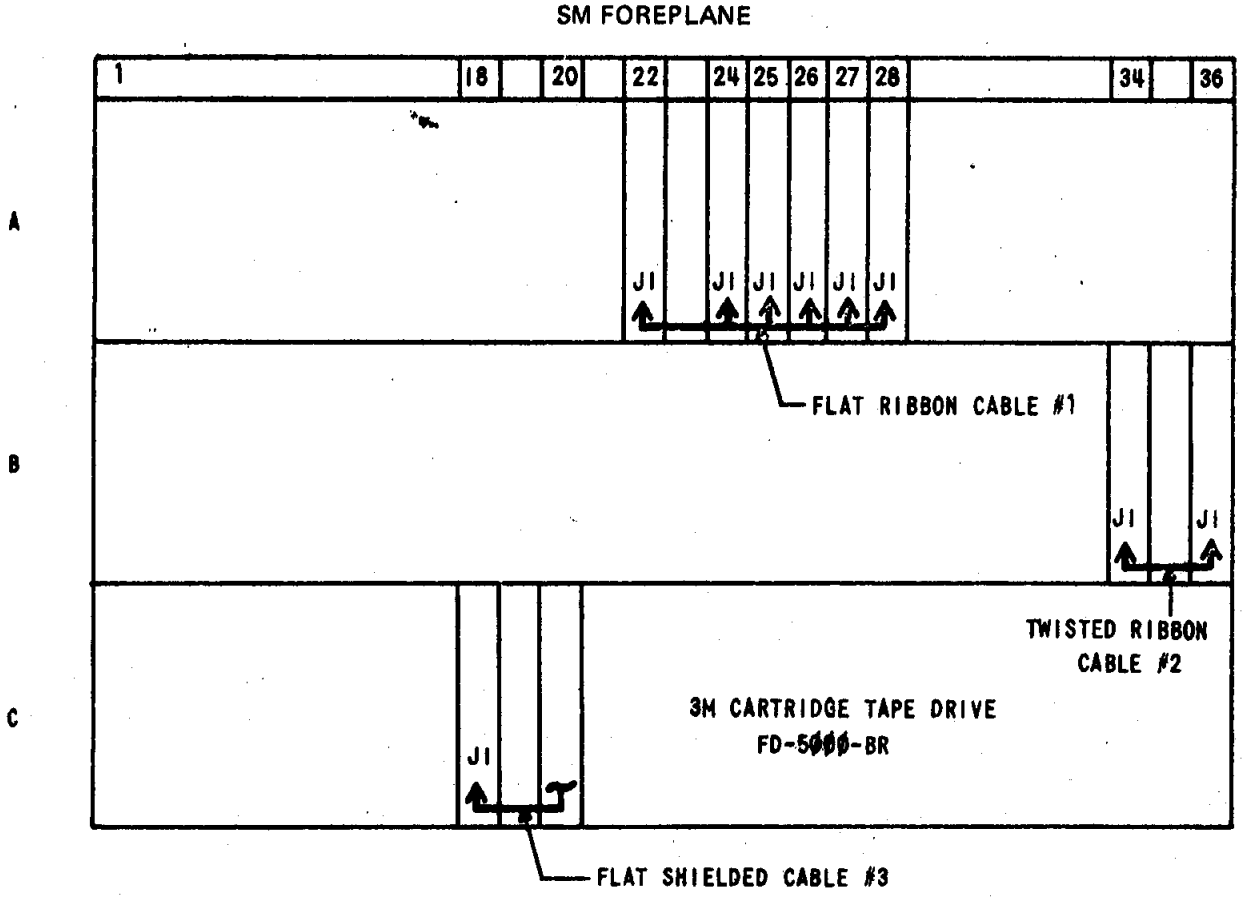
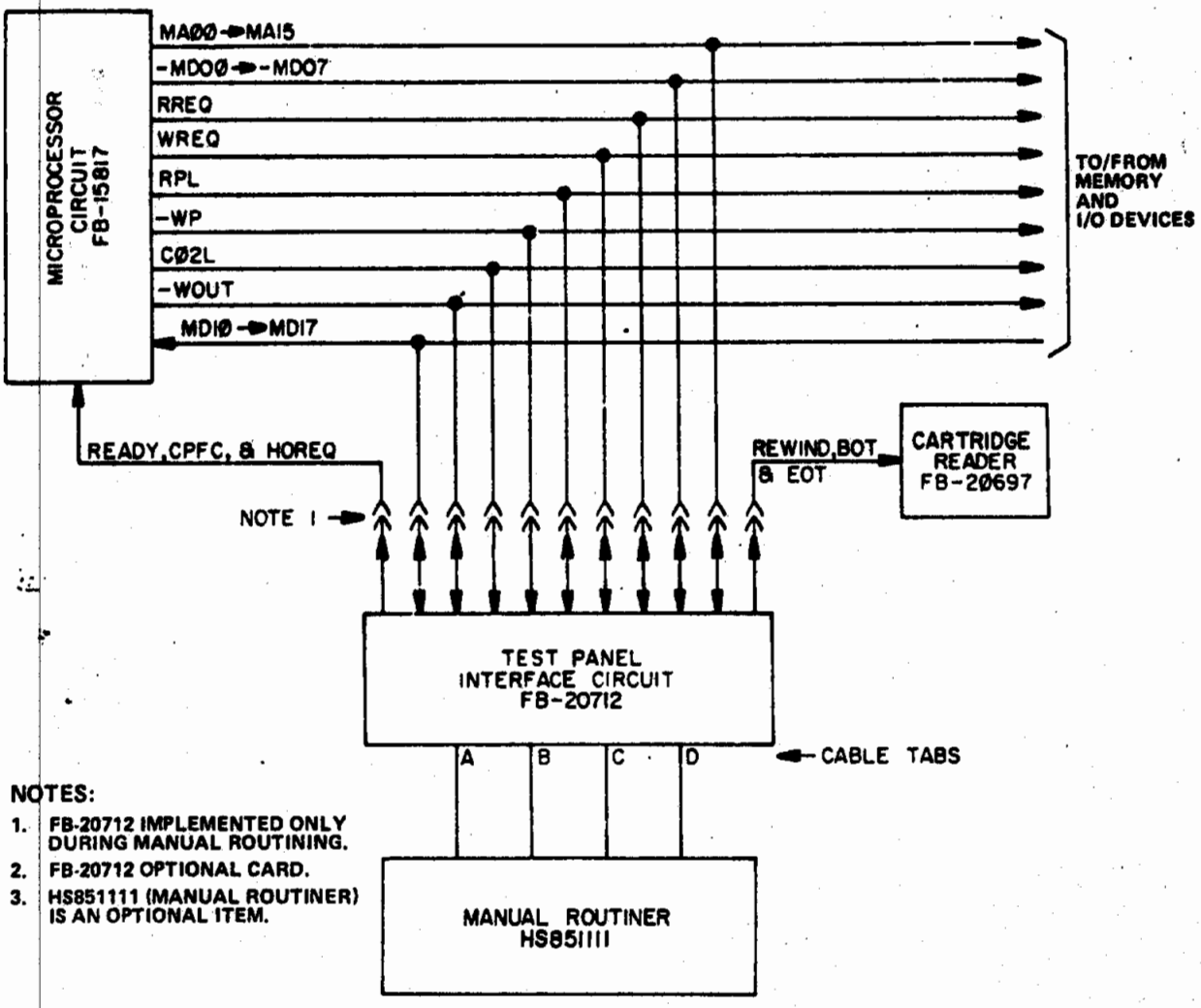


Figure 7. Internal SM Cabling.

00238

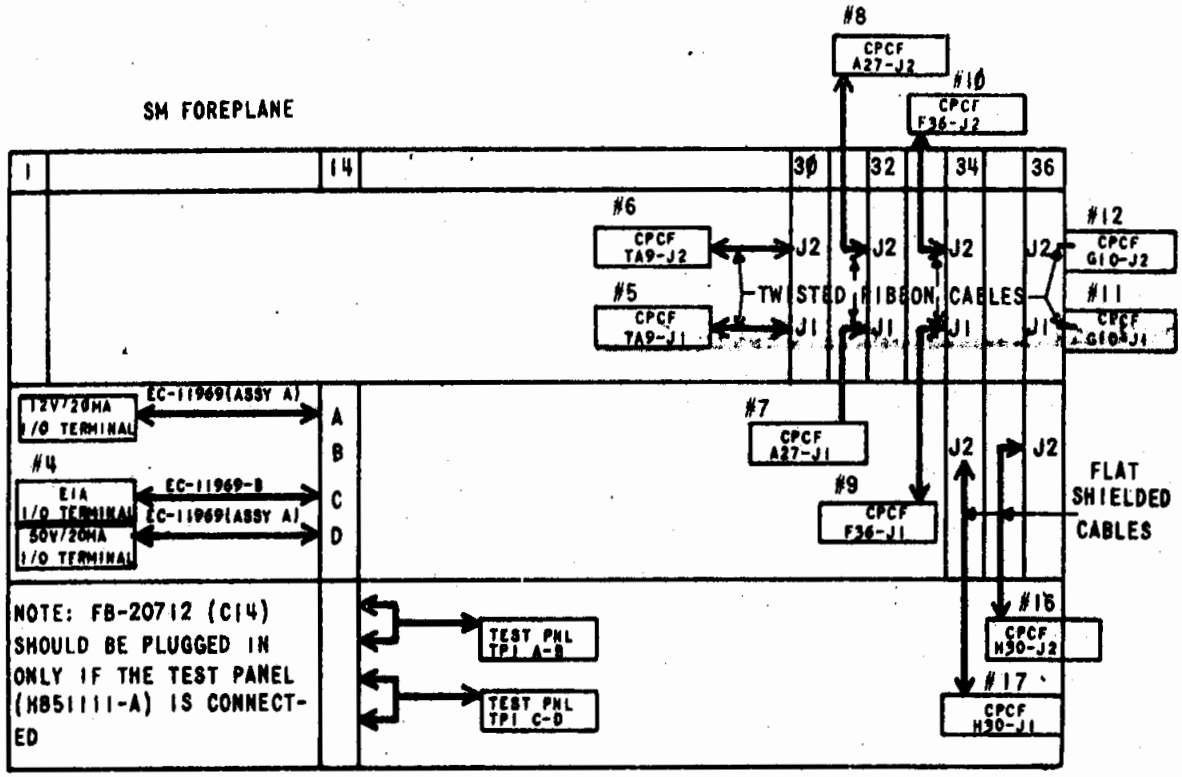


NOTES:

1. FB-20712 IMPLEMENTED ONLY DURING MANUAL ROUTINING.
2. FB-20712 OPTIONAL CARD.
3. HS851111 (MANUAL ROUTINER) IS AN OPTIONAL ITEM.

Figure 8. Test Panel Interface and Manual Routiner.

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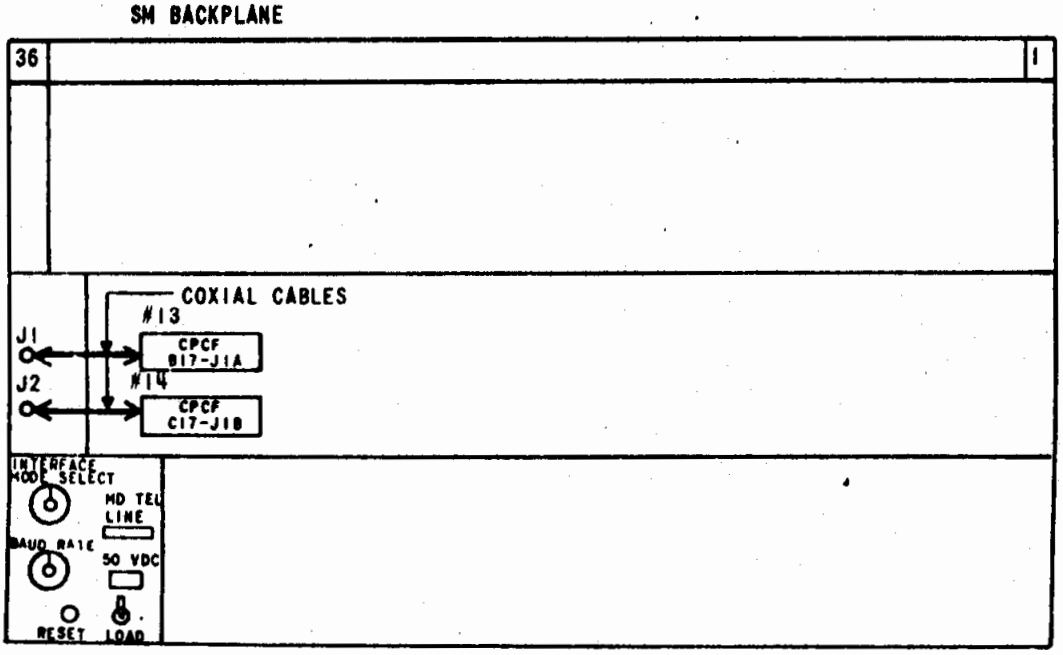
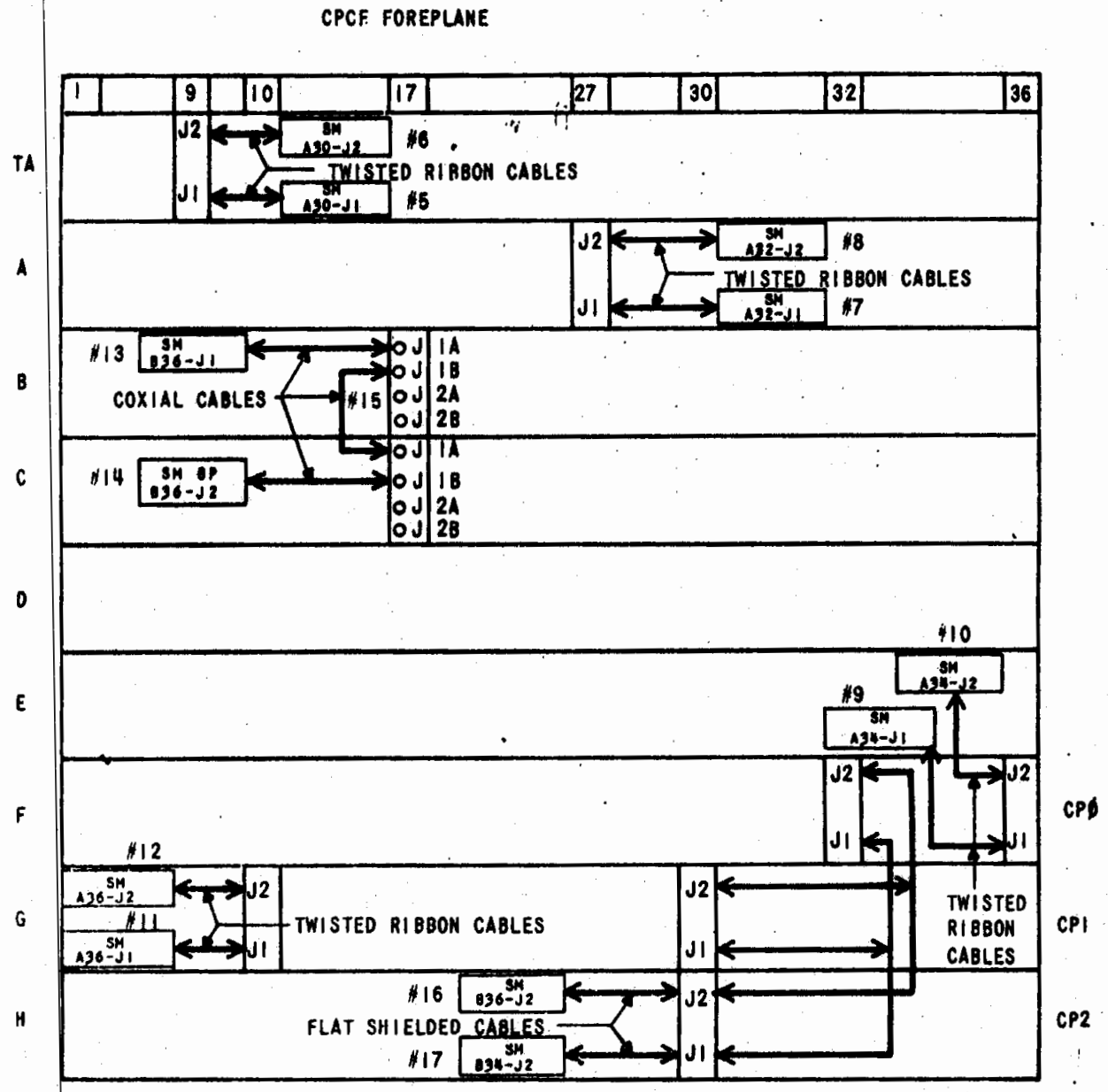


Figure 9. ~~Monitor~~ System Monitor ~~SM~~ -CPCF Cabling.



System Monitor

Figure 10. ~~Monitor~~ CPCF-SM Cabling

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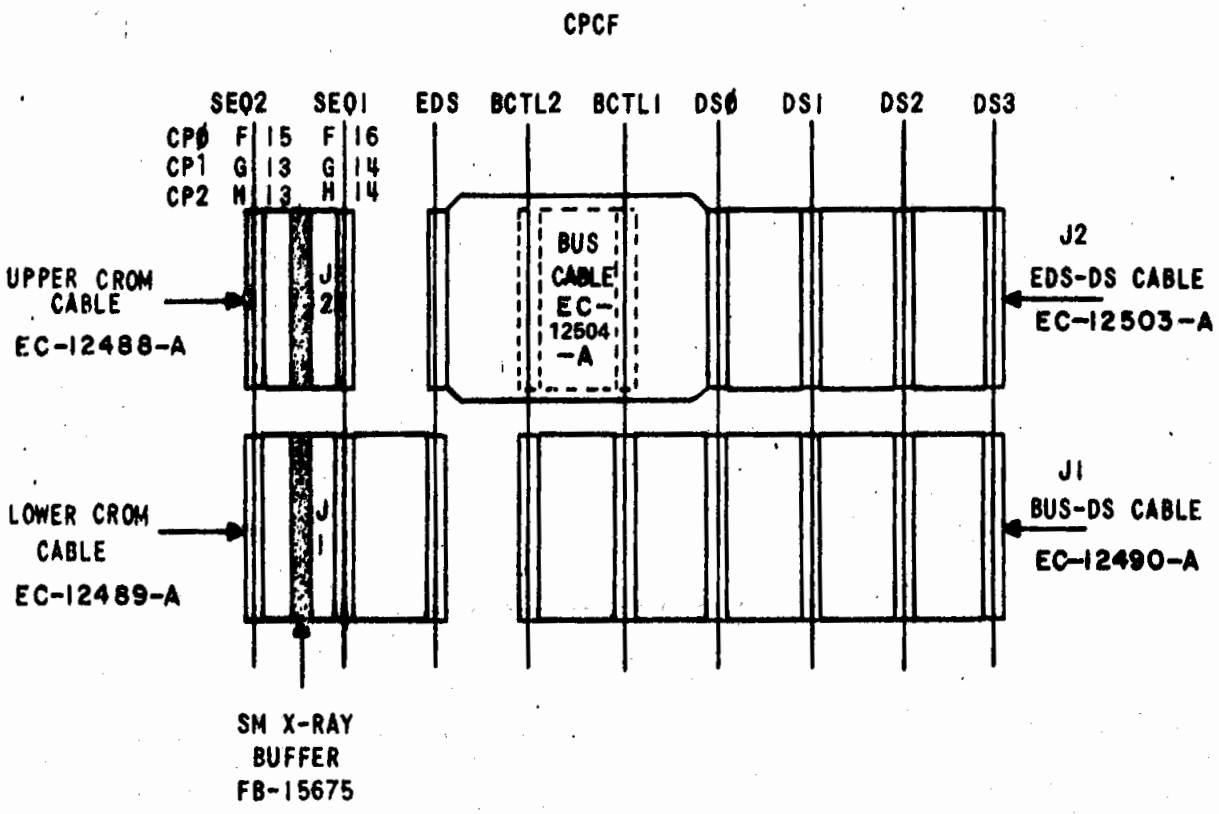


Figure 11. System Monitor X-ray Buffer Connection to CP.

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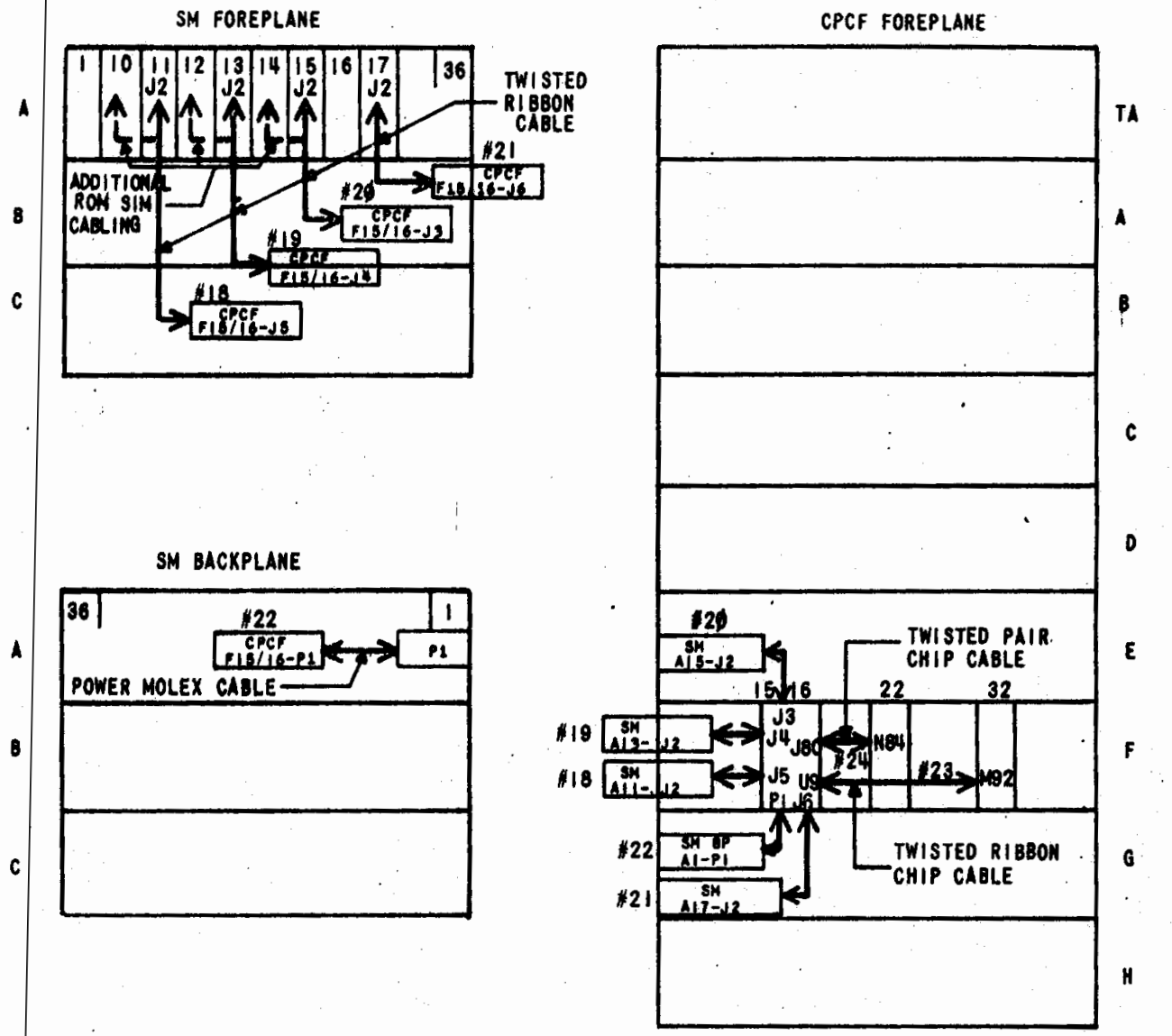


Figure 12. X-ray SM-CPCF (CPO) Cabling.

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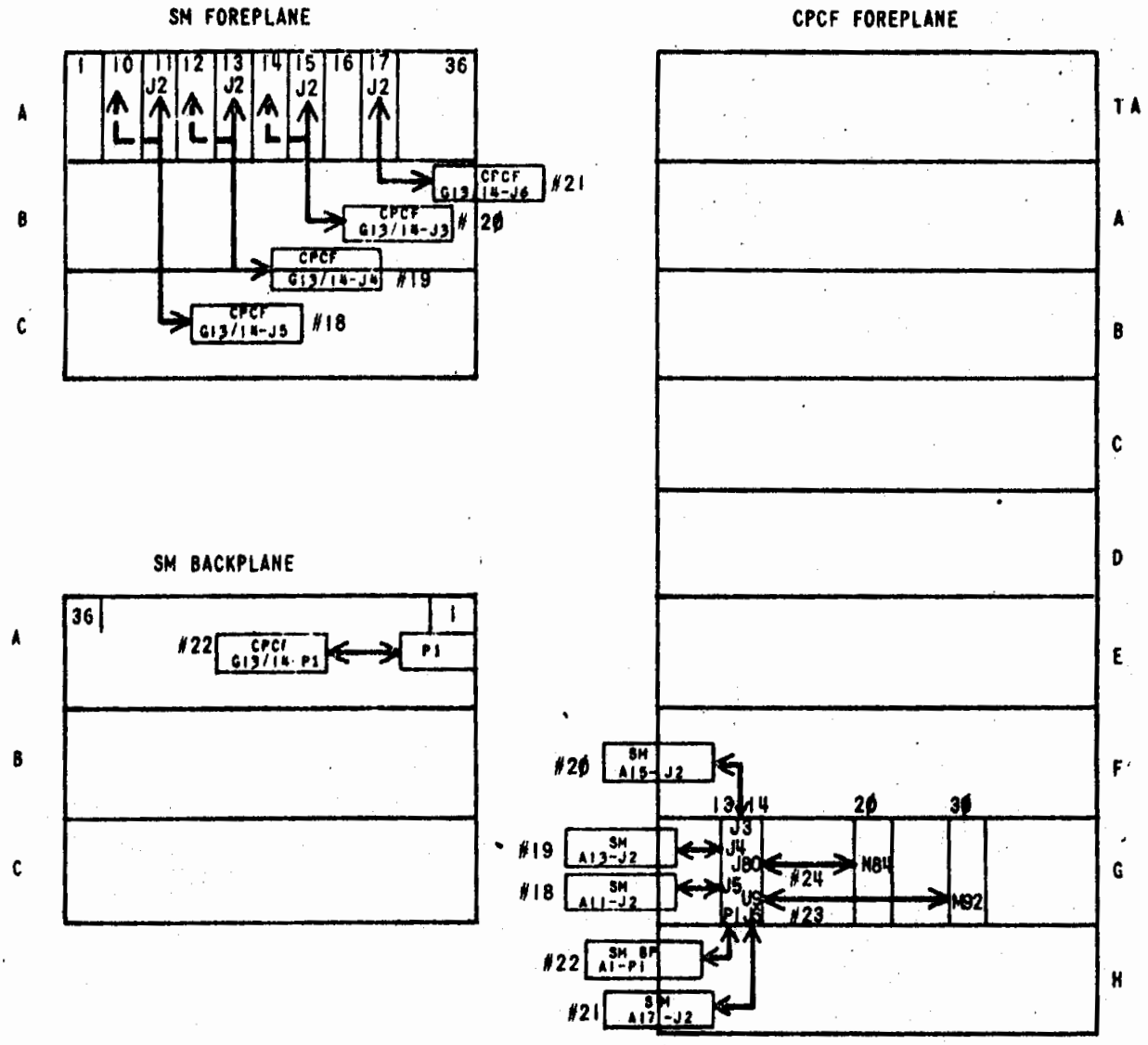


Figure 13. X-ray SM-CPCF (CP1) Cabling.

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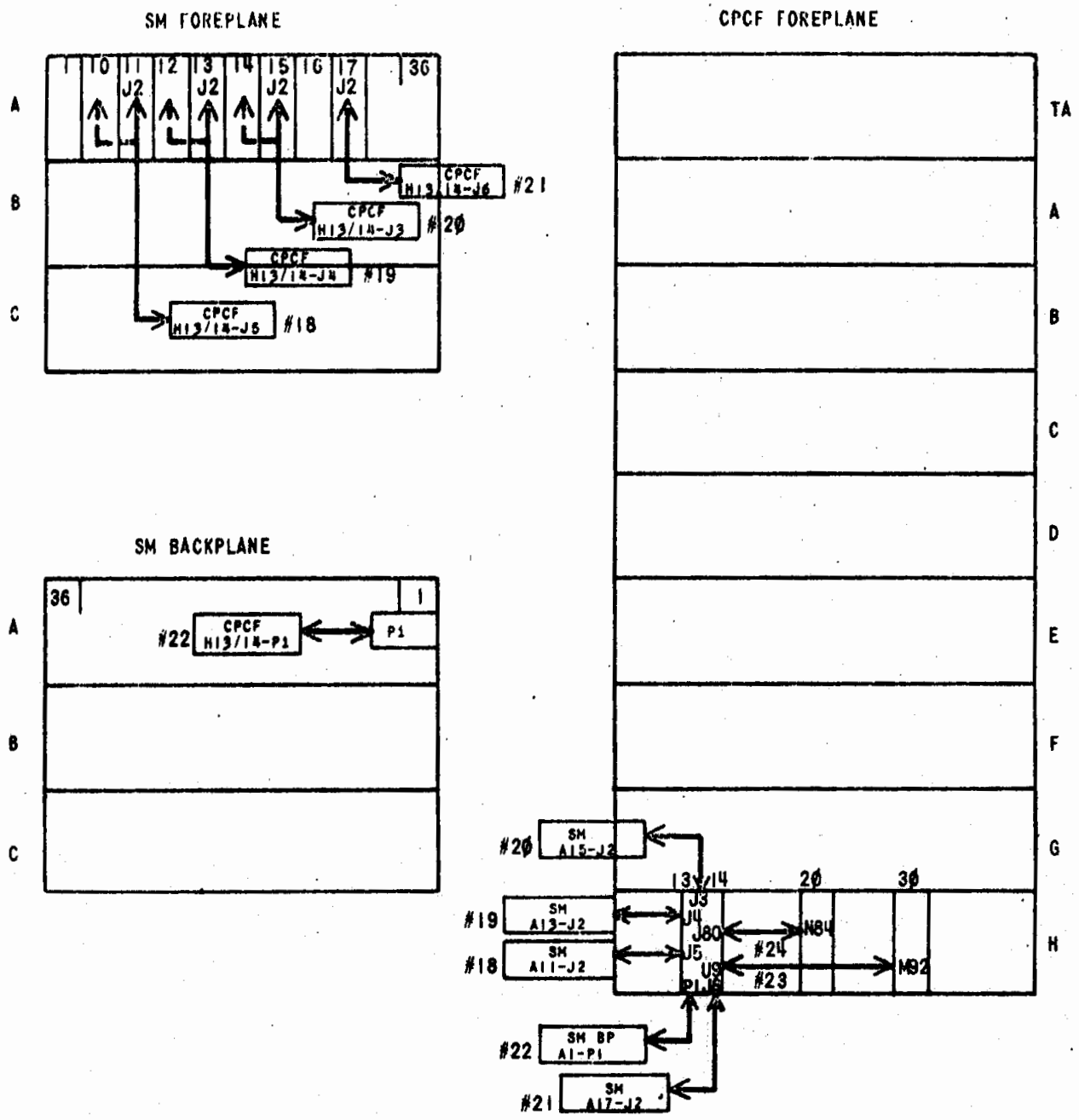


Figure 14. X-ray SM-CPCF (CP2) Cabling.

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TYPE 2B PROCESSOR COMPLEX CONTROL AND MEMORY COMPLEX INSTALLATION TEST PROCEDURES

CONTENTS

1. GENERAL

2. PREREQUISITES

3. TEST OBJECTIVES

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System Monitor Control and Memory Complex Interface
X-ray Execution
Memory Routining and Stabilization
Initial Program Load
Processor Control and Display Console and Control and Display Interface
Processor Control and Display Console and Control and Memory Complex Hardware Status

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Table 2. PCDC and MSAF Installation Test Procedure.

Table 3. System Monitor Bringup and CMC Interface Installation Test Procedure.

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Table 5. Memory Routining and Stabilization Installation Test Procedure.

Table 6. IPL Installation Test Procedure.

Table 7. PCDC and CDI Installation Test Procedure.

Table 8. PCDC and CMC Hardware Status Installation Test Procedure.

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Table 9. Dedicated Loader Input Parameters.

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LIST OF FIGURES

Figure 1. Typical Trace.

Figure 1a. Firmware Recovery Hardware Error Status Map.

Figure 1b. System Monitor Trace.

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1. GENERAL

1.01 This section provides the installation test procedures for the Type 2B Processor Complex Control and Memory Complex (CMC).

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500IT).

2.02 Test personnel should have access to the following documentation:

(a) Type 2B Processor Complex Engineering Configuration Document, 47-B-1018-0038.

(b) All FB- drawings for the Type 2B processor CMC.

(c) All FE- drawings for the Type 2B processor CMC.

(d) EL-15165.

(e) Section 227-200-300, Type 2B Processor Complex System Monitor - Description and Use.

(f) Section 227-201-502, Type 2B Processor Complex System Monitor - Static and Dynamic Installation Test Procedure.

(g) Section 227-200-301, Type 2B Processor Complex X-ray Program - Description and Use.

2.03 Test personnel should have access to the following equipment:

(a) The system monitor and all associated equipment and cabling.

(b) DC ammeter with a 0- to 15-ampere range.

(c) Carbon pile stack.

(d) Oscilloscope having a bandwidth dc to 200 MHz (HP 1725A or equivalent).

(e) Digital volt-ohm meter.

(f) One roll of daisy-chain backplane jumper wire.

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(g) Continuity tester (lamp or buzzer).

(h) System cable extractor tool.

(i) Card extender, FB-15403-A.

3. TEST OBJECTIVES

3.01 The objectives of the test procedures in this section is to bring up, test, and load the Type 2B processor CMC.

3.02 The three Central Processors (CP's) are initially tested in a simplex mode (using the system monitor X-ray programs), and a simplex path to the system Magnetic Tape Unit (MTU) is verified for the Initial Program Load (IPL). The untested CMC units are then tested using the X-ray programs.

4. TEST PROCEDURES

4.01 The initial bringup and testing of the CMC follows an orderly step-by-step procedure to alleviate unnecessary problems and delays in test time. In the X-ray mode, each CP is used to test itself, such that the X-ray programs verify internal processor functions in a sequential manner. (Deviation from the given sequence may cause unnecessary delays in testing.)

4.02 The IPL is accomplished with a fully operational system load, including CMC diagnostics that are used for more extensive CMC testing in a synchronous-triplex CP mode.

4.03 The CP's operate from internally decoded microinstructions received either from the Control Read-Only Memory (CROM) or the system monitor Read-Only Memory Simulator (ROMSIM). The system monitor X-ray microdiagnostic programs can only operate in a dynamic mode, and are to be sequentially executed to verify processor sanity from very basic to more complex functions. The programs are structured with pass/fail microaddresses and contain status and error information in the general registers. There are eight general registers numbered from 0 through 7. Analysis of X-ray program execution is accomplished

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by a system monitor trace that is manually set up before X-ray execution and analyzed after execution.

4.04 For analysis of hardware faults with the system monitor and X-ray programs, it is possible to have the X-ray program (with the selected phase in which the fault occurs) loop, such that an oscilloscope can be used for troubleshooting. The recommended procedure is to execute the selected X-ray program with all phases (tests) and all configuration parameters enabled. If a fault occurs consistently in a particular phase, the configuration parameters (if any) should be modified to isolate the fault to the faulty configuration only. The X-ray program will run continuously as long as the X-ray command is not input. To start the program running through the selected phase(s) and configuration(s), input the normal X-ray execute command.

4.05 If analysis of a particular fault requires an external trigger point for detection, it is possible to set up a hardware trigger (sync) point corresponding to a selectable microlocation (address). This microaddress can then be selected on the system monitor X-ray buffer card (FB-15675) that is connected to the CP through the foreplane and chip cables.

4.06 Sequentially perform the steps in Tables 1 through 8 to bring up and load the CMC. Tables 9 through 12 provide supplementary information, and are referenced in the test procedures where appropriate. If an error or problem occurs while performing the procedures, correct the problem and perform the associated step(s) again. Each procedure must be successfully completed before going on to the next table.

Initial Bringup

4.07 The procedure for bringing up the CMC is provided in Table 1. This procedure should be performed in the sequence given, without deviation, to verify proper operation of the CMC power supply system. If any abnormal

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result occurs, attempt to reproduce the condition and refer to the relevant EL-, FB-, and FE- drawings for specific information to correct the problem.

4.08 Central Processor and System Bus Cabling. The CP cabling should be performed in accordance with the Type 2B Processor Complex engineering configuration document, sheet 20. System bus cabling should be performed in accordance with sheet 3 of the same document.

4.09 Clock Coaxial Cabling. Backplane clock coaxial cabling should be performed in accordance with the Type 2B Processor Complex engineering configuration document, sheet 20.

NOTE: It is critical to system operation that all clock pairs be terminated. It may be necessary to connect any unused clock to a Memory Interface Unit (MIU) copy 1 terminator.

4.10 System Monitor and CMC Interface. The system monitor installation, self test, and CMC interface cabling should be performed in accordance with Section 227-201-502.

Processor Control and Display Console and Miscellaneous Status and Alarm Frame

4.11 Sequentially perform the steps in Table 2 for installation and testing of the Processor Control and Display Console (PCDC) and the Miscellaneous Status and Alarm Frame (MSAF).

System Monitor Bringup and Control and Memory Complex Interface

4.12 Sequentially perform the steps in Table 3 to bring up the system monitor and to verify proper system monitor and CMC interface.

X-ray Execution

4.13 Sequentially perform the steps in Table 4 to test and verify proper X-ray program execution.

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Memory Routining and Stabilization

4.14 To ensure stabilization prior to system software load and execution, the procedure in Table 5 provides for extensive exercising of memory. Sequentially perform the steps in Table 5 only after the CMC has been X-ray tested and is fully operational.

Initial Program Load

4.15 The procedure in Table 6 is completed for the IPL only after the complete X-ray program package has been successfully executed and the CMC is capable of executing system software.

4.16 In order to isolate possible hardware faults while attempting the IPL procedure and/or while executing system software, it is necessary to trace and accumulate data written into memory by firmware recovery. The relevant data is an assembled status of hardware errors that firmware recovery writes into a dedicated status area for use by diagnostic software.

4.17 The dedicated status area is structured such that different types of interrupts use their own dedicated area. Through the use of system monitor software trace capability, it is possible to capture this data while it is being written into memory by firmware recovery.

4.18 Connect the system monitor to the CMC for software monitoring. Refer to Section 227-201-502. Set up a system monitor trace for a Process-Store (PS) write of the firmware recovery status area. Refer to Section 227-200-300 and Figure 1 of this section for detailed information.

4.19 Sequentially perform the steps in Table 6 for the IPL.

Processor Control and Display Console and Control and Display Interface

4.20 Sequentially perform the steps in Table 7 to verify proper operation and interface of the PCDC and the Control and Display Interface (CDI) functional card.

00252

Processor Control and Display Console and Control and Memory Complex

4.21 Sequentially perform the steps in Table 8 to verify proper operation of the PCDC and firmware CMC status functions.

00253

Table 1. Initial Bringup Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Disconnect all cards, set all circuit breakers to OFF, and remove all fuses. Ensure that all backplane power bus cables are installed correctly.	
2	Inspect the 50-Vdc power cards for correct routing and termination. Inspect backplanes for bent and/ or broken pins and wires.	
3	Connect the frame power leads to the power feeder cable tops.	Power (50 Vdc) is applied to the frame.
4	Check for backplane power and ground shorts.	
5	Check the memory power bus between the Memory A frame/Memory B Frame (MEPF) and the Memory Power Frame (MEAF/MEBF) for shorts and continuity.	
6	On all FB-15228 card positions, strap the backplane OOS1 input (pin 31) to ground.	Control of frame power by use of the PWR REQ pushbutton is enabled.
7	Replace all 15-ampere fuses and set all circuit breakers to ON.	Power is applied to the backplane.

00254

Table 1. Initial Bringup Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
8	Check the polarity of -50 Vdc and ground on all backplane power plugs.	
9	Set all circuit breakers to OFF.	
10	Insert all equipped FB-15617 (Voltage Monitor (VM)) and FB-15228 (supervisory) cards into their respective positons.	
11	Replace all F2 and F3 fuses and ensure that all card FB-15228 PWR REQ pushbuttons are released.	On the FB-15228 cards, the OOS and PWR OFF lamps light. On the FB-15617 cards, the VM lamps light.
12	Insert all FB-15002, FB-15003, and FB-15004 cards into their respective positions. (Refer to document 47-B-1018-0038).	
13	Set all circuit breakers to ON.	
14	Depress the PWR REQ pushbutton on each FB-15228 card (for power on).	No fuses are blown. On the FB-15228 cards, the OOS and PWR ON lamps light. On the FB-15617 cards, the VM lamps go dark.
15	Depress the PWR REQ pushbutton on each FB-15228 card (for power off).	On the FB-15617 cards, the VM lamps light sequentially in desending numerical order.

00255

Table 1. Initial Bringup Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
	NOTE: Perform this step only for MEPF's. Skip to step 16 for other frames.	
16	Depress the PWR REQ pushbutton on each FB-15228 card (for power on).	On the FB-15617 cards, all VM lamps go dark. On the FB-15228 cards, the OOS and PWR ON lamps light.
17	Measure the voltage across ±TP on each FB-15617 card.	The voltage on each card is 1 ± 0.005 Vdc (adjustable).
18	Taking one fuse position at a time, insert a blown grasshopper fuse in each position on all FB-15228 cards.	On the FB-15228 cards, the UF lamps light.
19	Using the dc ammeter, digital volt-ohmmeter, and carbon pile stack, test all power supplies under rated loads. (Refer to the relevant FE-drawings for specific information).	
20	Using the dc ammeter, digital volt-ohmmeter, and carbon pile stack, test all power supplies for overload conditions.	The Power supply being tested has low resistance and a short circuit, and the VM lamps on the respective FB-15617 cards light.
	NOTE: Perform steps 21 through 28 only for MEPF's. For other frames, skip to step 26.	

00256

Table 1. Initial Bringup Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
21	Depress the PWR REQ pushbutton on each FB-15228 card (for power off).	On the FB-15228 cards, the PWR OFF and OOS lamps light, and the PWR ON lamps go dark. On the FB-15617 cards, the VM 8, 9, and 10 lamps light.
22	Disconnect the +5-Vdc power supply (card FB-15002 position 2). Depress the PWR REQ pushbutton on each FB-15228 card (for power on).	On the FB-15228 cards, the PWR OFF lamps light. On the FB-15617 cards, the VM 8 lamp lights, and after approximately 3 seconds, the VM 9 and 10 lamps light.
23	Repeat step 21.	The results correspond to those in step 21.
24	Disconnect the +12-Vdc power supply (card FB-15004, position 27). Depress the PWR REQ pushbutton on each FB-15228 card (for power on).	On the FB-15228 cards, the PWR OFF lamps light. On the FB-15617 cards, the VM 8 and 10 lamps light, and after approximataly 3 seconds, the VM 9 lamp lights.
25	Repeat step 21.	The results correspond to those in step 21.
26	Disconnect the -5-Vdc power supply (card FB-15003, position 6). Depress the PWR REQ pushbutton on each FB-15228 card (for power on).	On the FB-15228 cards, the PWR OFF lamps light. On the FB-15617 cards, the VM 8 and 10 lamps light, and after approximately 3 seconds, the VM 9 lamp lights.
27	Repeat step 21.	The results correspond to those in step 21.
28	Reconnect all power supplies (the power supplies disconnected in steps 22, 24, and 26).	On the FB-15228 cards, the PWR ON and OOS lamps light. On the FB-15617 cards, all VM lamps go dark.

00257

Table 1. Initial Bringup Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
29	Remove the OOS1 backplane strap (pin 31 to ground) from all FB-15228 cards (strapping was installed in step 6).	On all FB-15228 cards, the OOS lamps go dark.
30	With the circuit breakers still set to ON, remove the fuse from the FB-15004 power supply card.	The circuit breaker trips to OFF. On the FB-15617 cards, the VM lamps light. On the FB-15228 cards, the PWR OFF lamps light.
31	Replace the fuse in the FB-15004 card and set the tripped circuit breaker to ON.	On the FB-15617 cards, the VM lamps go dark. On the FB-15228 cards, the PWR OFF lamps go dark and the PWR ON lamps light.
	NOTE: The remainder of the steps in this procedure refer to terminal block TBA at the top of each frame. Refer to EL-15163-002 for pin numbers.	
32	Measure the voltage between the Out-Of-Service (OOS) lead on each FB-15228 card and ground on terminal block TBA.	The voltage between the OOS lead and ground is -50 Vdc.
33	With all PWR REQ pushbuttons on the FB-15228 cards released, measure for continuity between the REQ1 and REQ2 leads.	Continuity is present between the REQ1 and REQ2 leads.
34	On all FB-15228 card positions, strap the backplane OOS1 input to terminal block TBA ground.	Control of frame power by use of the PWR REQ pushbutton is enabled.

00258

Table 1. Initial Bringup Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
35	Measure for continuity between the PS1 and PS2 leads.	Continuity is present between the PS1 and PS2 leads.
36	Depress the PWR REQ pushbutton on each FB-15228 card. Then insert a blown fuse in each power supply and measure for continuity between the UF9 and UF10 leads.	Continuity is present between the UF99 and UF10 leads.
37	Measure for continuity between the GND lead and ground.	Continuity is present between the GND lead and ground.
38	Release the PWR REQ pushbutton on each FB-15228 card. Measure for continuity between the PS3 (negative) and PS4 leads.	Continuity is present between the PS3 and PS4 leads.
39	Invoke a unit fuse alarm by inserting a blown fuse in any power supply. Measure for continuity between the UF12 (negative) lead and ground.	Continuity is present between the UF12 lead and ground.
40	Depress the PWR REQ pushbutton on each FB-15228 card. Measure for continuity between the PONOFF A/B lead and ground.	Continuity is present between PONOFF A/B lead and ground.

00259

Table 1. Initial Bringup Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
41	Replace all fuses, depress (release) the PWR REQ pushbutton on each FB-15228 card (for power off), set all circuit breakers to OFF, and replace all FB-15228 OOS straps.	On the FB-15228 cards, the PWR OFF and OOS lamps light. On the FB-15617 cards, the VM lamps light.
42	Insert all equipped cards into their respective frame positions.	
43	Set all circuit breakers to ON.	
44	Depress the PWR REQ push-button on each FB-15228 card.	On the FB-15228 cards, the PWR OFF lamps go dark and the PWR ON and OOS lamps light. On the FB-15617 cards, the VM lamps go dark.

00260

Table 2. PCDC and MSAF Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Ensure that all frame cards are disconnected, that all circuit breakers are set to OFF, and that all fuses are removed.	
2	Inspect the 50-Vdc power cables for correct routing and termination.	
3	Inspect the file H backplane for bent and/or broken pins and wires.	
4	Connect the frame power leads to power feeder cable taps.	Power (50 Vdc) is applied to the frame.
5	Check for backplane power and ground shorts.	
6	Strap the backplane OOS1 input (in file H, slot 10 pin 31) to ground on card FB-15228.	Control of frame power by use of the PWR REQ pushbutton is enabled.
7	Insert 15-ampere fuses in rear fuse panel and file H, then set the circuit breaker in file H to ON.	Power is supplied to the fuse panel and the file-H backplane.
8	Check polarity of -50 Vdc and ground on all frame power plugs.	
9	Set both circuit breakers to OFF.	

00261

Table 2. PCDC and MSAF Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
10	Insert cards FB-15617 (VM) and FB-15228 (supervisory) into file H, slot 07 and file H, slot 10, respectively.	
11	Insert the F2 and F3 fuses into their proper frame positions, and ensure that the PWR REQ pushbutton on card FB-15228 is released.	On the FB-15228 card, the OOS and PWR OFF lamps light. On the FB-15617 card, the VM 10, 9, and 8 lamps light.
12	Insert cards FB-15002 and FB-15004 into file H, slot 01, and file H, slot 04, respectively.	
13	Set the file-H circuit breaker to ON.	
14	On the FB-15228 card depress the PWR REQ pushbutton (for power on).	No fuses are blown. On the FB-15228 card, the OOS and PWR ON lamps light. On the FB-15617 card, the VM lamps go dark.
15	Measure the voltage across ±TP on the FB-15617 card.	The voltage across ±TP is 1±0.005 Vdc (adjustable).
16	Taking one position at a time, insert a blown grasshopper fuse into each fuse position.	On the FB-15228 card, the UF lamp lights.

00262

Table 2. PCDC and MSAF Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
17	Using the dc ammeter, digital volt-ohmmeter, and carbon-pile stack, test the power supply under rated loads. (Refer to the relevant FE- drawing for specific information.)	
18	Using the dc ammeter, digital volt-ohmmeter, and carbon-pile stack, test the power supply for overload conditions.	The power supply has low resistance and a short circuit and the VM lamps on card FB-15617 light.
19	Remove the OOS backplane strap from the FB-15228 card (file H, slot 10, pin 31).	On the FB-15228 card, the OOS lamp goes dark.
20	With the file-H circuit breaker set to ON, remove the fuse from the FB-15004 power supply card.	On the FB-15228 card, the PWR OFF lamp lights. The file-H circuit breaker trips to OFF. On the FB-15617 card, the VM lamps light.
21	Replace the fuse in the FB-15004 card and set the file-H circuit breaker to ON.	On the FB-15617 card, the VM lamps go dark. On the FB-15228 card, the PWR ON lamp lights.
22	Depress the PWR REQ pushbutton on the FB-15228 card, set the file-H circuit breaker to OFF, and remove the 15-ampere fuse from file-H of the MSAF.	On the FB-15228 card, the OOS and PWR OFF lamps light. On the FB-15617 card, the VM lamps light.

00263

Table 2. PCDC and MSAF Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
23	On file G of the Central Processor Memory C Frame (CPCF), depress the PWR REQ pushbutton on the FB-15228 card and set the circuit breaker to OFF. Remove the 15-ampere fuse from file-D (right of the CPCF).	On the FB-15228 card, the OOS and PWR OFF lamps light. On the FB-15617 card, the VM lamps light.
24	Connect backplane power/ground bus cables from the MSAF, file-H backplane to the CPCF, file-H backplane.	
25	Connect signal cable from CPCF terminal board B to MSAF terminal board B.	
26	Check for continuity and shorts in the cable connections (steps 24 and 25).	
27	Replace the 15-ampere fuses in the CPCF, file-D (right) and the MSAF, file-H.	
28	Check for -50-Vdc and ground polarity.	
29	Connect the PCDC cable to MSAF terminal board 3.	
30	Set the circuit breakers in the CPCF, file-D (right) and the MSAF, file H to ON.	On the FB-15617 cards, the VM lamps light. On the FB-15228 cards, the OOS and PWR OFF lamps light.

00264

Table 2. PCDC and MSAF Installation Test Procedure (Continued),

STEP	OPERATION	RESULT/SYSTEM RESPONSE
31	On the FB-15228 cards in CPCF, file H and MSAF, file H, depress the PWR REQ pushbuttons (for power on).	On the FB-15228 cards, the OOS and PWR ON lamps light. On the FB-15617 cards, the VM lamps go dark.
32	Insert a 1.3-ampere grasshopper PCDC fuse in the MSAF fuse panel.	The indicator lamps on the PCDC light.

00265

Table 3. System Monitor Bringup and CMC Interface Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Perform the procedures for system monitor initial bringup and monitor cabling (Section 227-201-502).	
2	Force the selected CP (i.e., the CP to be X-ray tested) master by performing one of the following:	One of the following occur:
	(a) On the PCDC, depress the ENTRY START pushbutton and enter D via the keypad. Then simultaneously depress the FORCE XECUTE and MASTER STATUS CP pushbuttons.	(a) The PCDC display goes dark, the START pushbutton lights, and D is displayed. The EXECUTE, CPX, and CPY, Z (OOS) lamps light.
	(b) Strap the backplane for the selected CP. For CP0, strap file F, slot 16, pin 32 to GRND. For CP1, strap file G, slot 14, pin 32 to GRND. For CP2, strap file H, slot 14, pin 32 to GRND.	(b) If CP0 is master, the OOS CP1 and OOS CP2 lamps light. If CP1 is master, the OOS CP0 and OOS CP2 lamps light. If CP2 is master, the OOS CP0 and OOS CP1 lamps light.
3	Perform the procedures for system monitor self tests and X-ray cabling/ configuration (Section 227-201-502).	

00266

Table 3. System Monitor Bringup and CMC Interface Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
4	If the system monitor self-test and the buffer test (B TEST) continually fail for all buffer cards (i.e., no interrupt received during buffer write), and if the self-test for the microprocessor and operational Random Access Memory (RAM) have been successfully executed, examine and/or replace the coaxial clock cables and system monitor interface flat ribbon cables between the system monitor and the CMC.	

00267

Table 4. X-Ray Execution Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
	NOTE: The following procedure must be performed while referring to Section 227-200-301 because this section provides necessary general and detailed information on the X-ray programs and their operation.	
1	Ensure that CMC system cabling and system monitor/CMC X-ray cabling is correct.	
2	Execute the SEQTST, ALUTST, CLKTST, and TTEST programs.	The programs are successfully completed, with no known outstanding error conditions.
3	Disconnect the system bus cables from all Memory Interface Unit (MIU) cards.	Bus interference from the MIU's for initial access of Bus Interface Units (BIU's) is prevented.
4	Execute the BUSTST program. NOTE: It is recommended that each BUSTST program test be executed individually, and if necessary, that the refresh timer test be disabled when all tests are executed together.	The program is successfully completed with no known outstanding error conditions.
5	Connect the system bus cables for MIU0, copy 0 and copy 1.	
6	Execute the CRBTST, MTCTST, and CDITST programs.	The programs are successfully completed, with no known outstanding error conditions.

Table 4. X-Ray Execution Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
7	Disconnect the system bus cables from MIU0, copy 1. Load the MIUTST program into the system monitor ROMSIM.	
8	Set the parameters to MIU0, copy 0 only. Then set the high/low Unit Memory (MU) parameter to the lowest MU equipped.	
9	Execute the MIUTST program.	The program is successfully completed, with no known outstanding error conditions.
10	Set the high/low MU equipped input parameter to the next equipped MU and repeat step 9.	The MIUTST program is successfully completed, with no known outstanding error conditions.
11	Repeat step 10 for each equipped MU.	The results correspond to those in step 10.
12	Connect the system bus cables to copy 1. Set the input parameters to MIU0, copy 1, and the high/low MU parameter to the lowest MU equipped.	
13	Repeat steps 9 through 11.	The results correspond to those in steps 9 through 11.
14	Connect the system bus cables for the next equipped MIU copy, and repeat steps 8 through 13 for all equipped MIU's.	The results correspond to those in steps 8 through 13.

00269

Table 4. X-Ray Execution Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
	NOTE: At this stage of the X-ray execution procedure, all system bus cables should be connected to their respective terminations.	
15	Execute the MUTEST program for all equipped MU's. NOTE: It is recommended that memory be routined by executing the MUTEST program continuously for 8 error-free hours.	The program is successfully completed, with no known outstanding error conditions.
16	Execute the BIUTST program.	The program is successfully completed, with no known outstanding error conditions.
17	Ensure correct cabling and configuration between the CMC (PAU), NPCF (PCU), and IOAF (PUM).	
18	Using input parameters for the cabling/configuration verified in step 17, execute the PAUTST program.	The program is successfully completed, with no known outstanding error conditions.
19	Perform the static test for the magnetic tape transport.	The test is successfully completed with no known outstanding error conditions.
20	Execute the MTUTST program.	The program is successfully completed, with no known outstanding error conditions.

00270

Table 4. X-Ray Execution Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
21	Ensure correct cabling and configuration for all equipped Peripheral Controllers (PC's).	
22	Using the input parameters for the cabling/configuration verified in step 21, execute the PAUTST program for each individual PC (for non-network matrices only).	The program is successfully completed, with no known outstanding error conditions.
23	Execute the GRNEPCTST, STKTST, AND DCDTST programs.	The programs are successfully completed, with no known outstanding error conditions.
24	Repeat steps 1 through 23 for the untested CP copies, except do not perform those steps that call for disconnection of the system bus cables (i.e., steps 3 and 7). NOTE: Using system X-ray programs, test all spare CMC printed wiring cards before preforming the next procedure.	The results correspond to those in steps 1 through 23.

00271

Table 5. Memory Routining and Stabilization Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
	NOTE: For the general and detailed information necessary for the performance of this test, refer to Section 227-200-301.	
1	Load the MUTEST program into the system monitor ROMSIM.	
2	Use the X-ray phase select parameter to select MUTEST phases 0 (initialization) and 2 (all 0's test).	When the program is executed, the CMC will be initialized and memory read/write operations will be performed using in all-0's data pattern.
3	Use the X-ray parameter control to reflect all equipped memory.	
4	Execute the MUTEST program in the normal X-ray mode.	The program is successfully completed, with no known outstanding error conditions.
5	Input the following to use the X-ray inspect and change capability to disable the memory write functions: CONTROL-C (STX) X-RAY X-RAY (S,L,E,EM,I,T,P,G) = I 30A (for all 0's test) 310 (for all 1's test) 316 (for addressing test) 000000000000 for all tests	The terminal outputs **X-RAY** X-RAY INSPECT ADDRESS = 030A 1600000000 91- 031A 1600000000 91- 0316 1600000000 91-

00272

Table 5. Memory Routining and Stabilization Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
6	Execute the MUTEST program (performing only the read operations, comparing memory contents to the data pattern written by the previous execution).	The program is successfully completed, with no known outstanding error conditions.
7	Do not input any further X-ray commands. (Doing so would force the CP to microlocation 0 and stop the CP). Allow the system to remain in this configuration for a period of 2 to 8 hours.	The CMC remains idle, with only the memory refresh being automatically executed.
8	Execute the MUTEST program, using a different phase(s) than that specified for execution in step 5.	The program is successfully completed, with no known outstanding error conditions.
9	Repeat steps 1 through 8, executing all remaining phases of the MUTEST program.	The results correspond to those in steps 1 through 8.

00273

Table 6. IPL Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Mount the system generic tape or composite tape on the Input/Output Access Frame (IOAF) Magnetic Tape Unit (MTU). NOTE: Ensure that the write enable ring is removed from the tape before mounting, or an error will result when attempting IPL.	
2	Ensure that the MTU is on-line, and that the tape is at Beginning of Tape (BOT).	
3	On the PCDC, depress the ENTRY START push-button.	On the PCDC, the display goes dark, and the ENTRY START pushbutton lights.
4	Using the PCDC keypad, enter the load parameter digits (i.e., enter abcdeefg). Refer to Table 7 for load parameter digits definitions.	The PCDC displays abcdeefg where abcdeefg = load parameter digits
5	Simultaneously depress the FORCE XCUTE push-button and the push-buttons associated with the selected CP.	The FORCE XCUTE pushbutton lights. The tape load begins.

00274

Table 6. IPL Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
6	Depress the ENTRY START pushbutton. Then simultaneously depress the FORCE XCUTE pushbutton and the pushbuttons associated with the selected CP (the same pushbuttons depressed in step 5).	On the PCDC, the display goes dark, the ENTRY START pushbutton lights, and the FOREC XCUTE pushbutton goes dark (master force is removed from the selected CP).
7	Wait for tape load to complete.	When the tape load is successfully completed, the PCDC displays TAPE IS LOADED
	NOTE: If the tape load is successful, and if no other tapes are required for the system load, skip steps 8 through 13 and perform step 14. If the tape load is successful, and if tapes are required for the system, skip steps 8 and 9 and perform step 10. If the tape load is not successful, continue this procedure starting with step 8.	
8	If an error is encountered during tape loading (i.e., if the PCDC displays DXXX), refer to Table 8 for definitions of dedicated loader error messages.	
9	Correct the problem identified in step 8, then repeat steps 1 through 7.	The results correspond to those in steps 1 through 7.
10	Remove the successfully loaded tape from the MTU.	

00275

Table 6. IPL Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
11	Repeat steps 1 through 4. NOTE: If desired, a different MTU with different loading parameters may be used.	The results correspond to those in steps 1 through 4.
12	On the PCDC depress the FUNCTIONS DATA FCN pushbutton.	The tape load begins.
13	Repeat steps 6 and 7 and, if necessary, steps 8 and 9.	The results correspond to those in steps 6 and 7, and 8 and 9.
14	On the PCDC depress the ENTRY START pushbutton.	On the PCDC, the display goes dark and the ENTRY START pushbutton lights.
15	Using the PCDC keypad, enter the digit 4.	The PCDC displays the digit 4.
16	On the PCDC simultaneously depress the FORCE XCUTE and INIT pushbuttons.	On the FORCE XCUTE and INITIALIZATION pushbuttons light LOAD COMPLETE is displayed.
17	On the PCDC depress the CLEAR pushbutton.	The PCDC displays the percentage of software execution. After approximately 2 minutes, the INIT pushbutton goes dark, and the system terminal outputs SIA LEVEL 4 INITIALIZATION COMPLETED

00276

Table 7. PCDC and CDI Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Ensure the following conditions exist: (a) All cabling is installed correctly. (b) All power is on, with no alarms. (c) All cards are inserted in the correct positions.	
2	On file H of the MSAF, depress and then redepress the PWR REQ pushbutton on card FB-15228 (for power off and power on, respectively).	The CDI circuitry in CPCF, file H is reset and cleared.
3	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, ENTRY START pushbutton lights.
4	On the PCDC keypad, enter 11.	The PCDC displays 11.
5	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	The PCDC displays *ABCDEFGHIJKLMNOPQRSTUVWXYZ[]{}?
6	On the PCDC, depress the CLEAR pushbutton.	The PCDC display goes dark.
7	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, the ENTRY START pushbutton lights.
8	On the PCDC keypad, enter 12.	The PCDC displays 12.

00277

Table 7. PCDC and CDI Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
9	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	The PCDC displays 0123456789@ = ;/.!-"#$%(')+,:
10	On the PCDC, depress the ENTRY START pushbutton.	The PCDC display goes dark and the ENTRY START pushbutton lights.
11	On the PCDC keypad, enter 13.	The PCDC displays 13.
12	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	On the PCDC, the CE MAJ, INIT, FUNCTIONS DATA FCN, CLOCK MIN, DMA MAJ, PERIF MAJ, and MEMORY MAJ lamps light and the MONITOR SIA, FUNCTIONS MCS, CE MIN, DMA MIN, PERIF MN, and MEMORY MIN lamps go dark. The firmware recovery, software recovery, and reload indicators remain unchanged.
13	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, the ENTRY START pushbutton lights. The PCDC display goes dark.
14	On the PCDC keypad, enter 14.	The PCDC displays 14.
15	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	On the PCDC, the MONITOR SIA, FUNCTIONS MCS, CE MIN, DMA MIN, PERIF MIN, and MEMORY MIN lamps light and the CE MAJ, INIT, FUNCTIONS DATA FCN, CLOCK MIN, DMA MAJ, PERIF MAJ, and MEMORY MAJ lamps go dark.
16	The the PCDC, depress the ENTRY START pushbutton.	The PCDC display goes dark and the ENTRY START pushbutton lights.

00278

Table 7. PCDC and CDI Installation Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
17	On the PCDC keypad, enter 15.	The PCDC displays 15.
18	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	The PCDC display and lamps return to a normal pre-test state.
19	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, the display goes dark and the ENTRY START pushbutton lights.
20	On the PCDC keypad, enter 16 followed by any other six digits (for example, 16 24A6F9).	The PCDC displays 16 and the six digits entered.
21	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	The PCDC display changes, dropping 16 and displaying only the six other digits.
22	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, the display goes dark and the ENTRY START pushbutton lights.
23	On the PCDC keypad, enter 17 followed by a two-digit hexadecimal code.	The PCDC displays 17 and the two-digit code.
24	On the PCDC, depress the FUNCTIONS DATA FCN pushbutton.	On the PCDC, the character associated with the two-digit code entered in step 23 is displayed 32 times.
25	On the PCDC, depress the CLEAR pushbutton.	The PCDC display returns to normal.

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Table 8. PCDC and CMC Hardware Status Installation Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Verify the status of each CMC unit from the PCDC. Refer to Table 11 for definitions of input parameters.	
2	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, the display goes dark and the ENTRY START pushbutton lights.
3	On the PCDC keypad, enter D00cd(e/f) Refer to Table 11 for definitions of the variables c, d, e, and f.	The PCDC displays D00cd(e/f)
4	On the PCDC, depress the DATA FCN pushbutton.	On the PCDC, the ENTRY START pushbutton goes dark, the FIRM RCVR lamp flashes, and one of the following is displayed: (a) STATUS XX (b) STATUS REJECTED YYY Refer to Table 12 for output status (XX) and input rejection code (YYY) definitions.
5	Repeat steps 2 through 4 for all equipped CMC units and copies.	The results correspond to those in steps 2 through 4.

Table 9. Dedicated Loader Input Parameters.

VARIABLE	MEANING	VALUE/FUNCTION
a	Bus availability	0 = Bus 0 1 = Bus 1 2 = Both buses (0 and 1)
b	PIU availability	0 = PIU0 1 = PIU1
c	ISO location	0 = MU0.0.0 1 = MU1.0.0 2 = MU*.0.0
d	PC number	
ee	PC matrix number	
f	Routining, load, and bypass indicators	For 9111(FL2): 0 = Routining, no load. 1 = No routining, load current map, no bypass. 3 = No routining, load current map, bypass read/write check. 5 = No routining, load current map, bypass tape errors. 7 = No routining, load current map, bypass read/write check and tape errors. 9 = No routining, load FOD map, no bypass. B = No routining, load FOD map, bypass read/write check. D = No routining, load FOD map, bypass tape errors. F = No routining, load FOD map, bypass read/write check and tape errors.

00281

Table 9. Dedicated Loader Input Parameters (Continued).

VARIABLE	MEANING	VALUE/FUNCTION
		For 9020(FL1): 8 = Routining, no load. 0 = No routining, load FOD map, no bypass. 1 = No routining, load FOD map, bypass read/write check. 2 = No routining, load FOD map, bypass tape errors. 3 = No routining, load FOD map, bypass read/write check and tape errors.
g	Update tape indicators	0 = No update. 1 = Update, forward mode, no override. 3 = Update, reverse mode, no override. 5 = Update, forward mode, override old data. 7 = Update, reverse mode, override old data.

00282

Table 10. Dedicated Loader Error Messages.

MESSAGE	MEANING
D004	Tape is stuck in forward mode.
D005	Transport not ready.
D006	Not real mode.
D008	Rewind error.
D009	Reverse error.
D00A	Buffer not ready.
D00B	Buffer overrun.
D00C	Tape mark found.
D00D	Output not ready.
D00E	Tape parity error.
D00F	Bad record type.
D010	No end record.
D011	Bad check sum.
D014	Address out of range.
D016	Memory error.
D017	Wrong tape.
D018	Scatter tape format.
D019	Update mismatch.
D01A	Implementation error.
D01B	Load will not verify.
D0FF	FL2 memory error.

00283

Table 11. Input Status Identifiers.

VARIABLE	VALUE	MEANING
a	0	Check status
	1	Put change status
	5	Force change status
b	0	Status check
	1	OOS.RCVY
	2	OOS.TEST
	3	OOS.TEMP
	4	OOS.SYS
	5	OOS.MM
	6	Precut
	7	Not Equipped
	8	INS. SBY
	9	INS.ACT
	A	INS.RTN
	B	INS.IDLE
	C	INS.BSY
	D	INS.CMPN
	E	INS.TEST
	F	INS
c	0	CP
	1	Bus
	2	MU
	3	PC
	4	MIU
	5	PIU
	6	PCDC
	7	CM
	8	RM
	9	PCLK
	A	CPPZ
	B	MPZ
	C	PIPZ
d	COPY	CP, Bus, PIU CM, RM
	PIU COPY	PIPZ
	MEMORY COPY	MPZ

00284

Table 11. Input Status Identifiers (Continued).

VARIABLE	VALUE	MEANING
e	SET UNIT BUS COPY	MU, MIU, MPZ PC PIPZ
f	UNIT BUS COPY	MU MPZ

00285

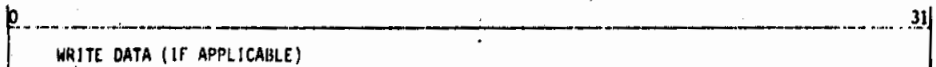
Table 12. Output Status and Input Rejection Code Definitions.

VALUE	DEFINITION
	OUTPUT_STATUS (XX)
01	OOS.RCVY
02	OOS.TEST
03	OOS.TEMP
04	OOS.SYS
05	OOS.MM
06	Precut
07	Not Equipped
08	INS.SBY
09	INS.ACT
10	INS.RTN
11	INS.IDLE
12	INS.BUSY
13	INS.CMPN
14	INS.TEST
15	INS
	INPUT REJECTION CODES (YYY)
72	Call register not available
73	OOS limit exceeded
74	Pre-job command invalid
75	Power off unit
76	Invalid status change
77	No standby copy
78	Invalid hardware identifier
79	Invalid unit address
80	Configuration restraint
81	Test unit not available
82	Post-job command invalid
286	Camp-on timer expired
320	Hardware not accessible

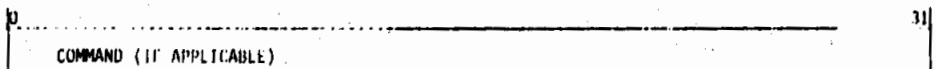
00286

TYPE OF INTERRUPT	STATUS AREA (FOR FLI)
RECURSION	P.S.PO + "10C0"
HARDWARE	P.S.PO + "10E0"
SOFTWARE/FIRMWARE	P.S.PO + "1140"
PCIOC	P.S.PO + "1140"
CLOCK	P.S.PO + "1180"

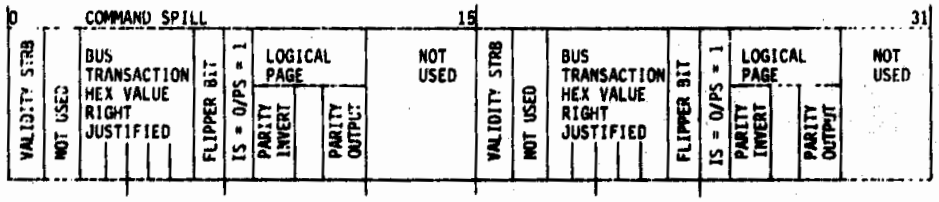
STATUS AREA + "B"



STATUS AREA + "C"



STATUS AREA + "D"

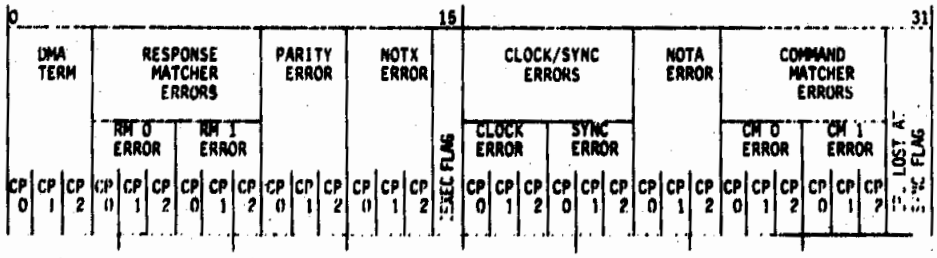


BUS TRANSACTION (BAD BITS) DECODE

01 = DMA WRITE DATA	08 = MAPPED READ	12 = UNMAPPED READ	19 = PAU RETURN				
02 = MAPPED FETCH	09 = MAPPED WRITE	13 = UNMAPPED WRITE	1A = DATA CR TO BHIST				
03 = WRITE DATA FLIPPED	0A = DMA DR TO BHIST	14 = MAPPED FETCH SR	1B = WRITE DATA EP				
04 = MAPPED FETCH EXEC	0B = WRITE DATA	15 = REFRESH	1C = ACCESS PAU SR				
05 = PIPELINE	0C = MAPPED READ SR	16 = MAPPED DMA READ	1D = MAPPED WRITE UNP				
06 = MAPPED FETCH(ALU=0)	0D = MAPPED WRITE SR	17 = MAPPED DMA WRITE	1E = READ MAP				
07 = MAPPED FETCH(ALU=0)	10 = DMA ORDER	18 = ACCESS PAU	1F = WRITE MAP				

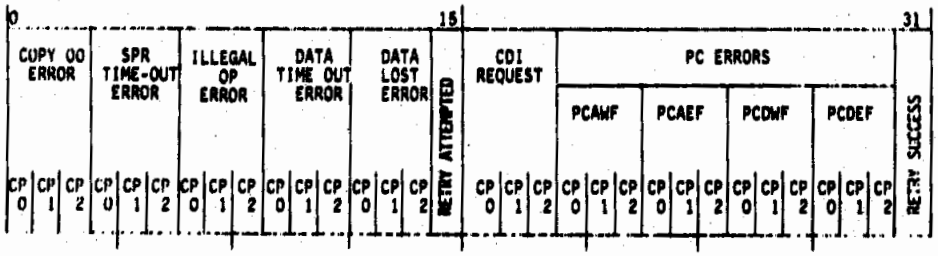
ASSEMBLED CPU ERROR WORD 1

STATUS AREA + "E"



ASSEMBLED CPU ERROR WORD 2

STATUS AREA + "F"



PC ERROR DEFINITION

PCAWF = PC ADDRESS ASW FAILURE
PCAEF = PC ADDRESS ECHO FAILURE
PCDWF = PC DATA ASW FAILURE
PCDEF = PC DATA ECHO FAILURE

Figure 1a Firmware Recovery Hardware Error Status Map.
Figure 1. Typical Trace.

```
I* TRACE

**TRACE**
1 COPY (0,1,B) = B
2 MODE (P,R) = P
3 TYPE (IS,PS,PC,INS,XFR,MEM,DMA,CMD)=PS
READ-WRITE (R,W,B) = W
4 START (ADDR,EXT,IMMED) = ADDR
START ADDR = R010C0:01180
EVENT CAPTURE (A,Q) = Q
DATA =
5 STOP(ADDR,EXT,OVFL)=0
6 IAR =
EVENTS = 17
READY (Y,N,E,X,A) = Y
** MONITOR ** V1.2

1* STOP (NECESSARY TO SIMULATE BUFFER OVERFLOR)

** MONITOR ** V1.2

LINE EVENTS    IAR       R/W-ADR    DATA       OP   TYP
                                                      R/W-ADR INDICATES A
0001 0017      04104     01100      0F090000   00   01   SOFTWARE/FIRMWARE INTERRUPT
0002           04104     01101      00080000   100  01
0003           04104     01102      12590000   100  01
0004           04104     01103      00200000   100  01
0005           04104     01104      C0000000   100  01
0006           04104     01105      00070000   100  01
0007           04104     01106      00060007   100  01
0008           04104     01107      01470CC4   100  01
0009           04104     01108      01474104   100  01
000A           04104     01109      DE840040   100  01
000B           04104     0110A      0030CF0F   100  01
000C           04104     0110B      00004105   100  01 - WRITE DATA: N/A
000D           04104     0110C      00000000   100  01 - COMMAND: N/A
000E           04104     0110D      00000000   100  01 - COMMAND/DATA SPILL: N/A
000F           04104     0110E      00000000   100  01 - CPU ERR WORD 1: NO ERRORS
0010           04104     0110F      00100000   100  01 - CPU ERR WORD 2: CP2 DATA TO
0011           04104     01110      0030CF0F   100  01
0012           04104     01111      DE800000   100  01
0013           04104     01112      00000000   100  01
0014           04104     01113      00000008   100  01
0015           04104     01114      01470CC4   100  01
0016           04104     01115      00000000   100  01
0017           04104     01116      DC2A004E   100  01


** MONITOR ** V1.2
```

Figure 1b. System Monitor Trace .
Figure 1. Typical Trace .

SECTION 227-203-501

Final System 6 copy

TYPE 2B PROCESSOR COMPLEX
CENTRAL PROCESSOR AND ASSOCIATED UNITS STATUS
INSTALLATION TEST PROCEDURES

CONTENTS

1. GENERAL

2. PREREQUISITES

3. TEST OBJECTIVE

4. TEST PROCEDURES

List of Tables

Table 1. Central Processor Status Test Procedure.

Table 2. Bus Status Test Procedure.

Table 3. Command Matcher and Response Matcher Status Test Procedure.

Table 4. Clock Status Test Procedure.

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1. GENERAL

1.01 This section provides the installation test procedures for testing the status, controls, and indications for the Central Processor (CP), bus, Command Matcher (CM), Response Matcher (RM), and clock portions of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the following conditions exist prior to performing the test procedures in this section:

(a) All Type 2B Processor Complex units are free of faults and in service.

(b) The system configuration is in the full-duplex mode with all copies 0 primary.

(c) All switches and pushbuttons on the Processor Control and Display Console (PCDC) are in their normal or unoperated position.

(d) All lamps on the SYSTEM STATUS AND ALARM subpanel of the Status and Alarm Panel (SAP) are unlit.

(e) One terminal is available for maintenance inputs.

(f) Section 227-201-502, System Monitor - Static and Dynamic Installation Test Procedure, has been successfully completed.

(g) A level 2 initialization has been manually generated from the PCDC.

2.03 Test personnel should have access to the following documentation:

(a) The Input/Output Message Manual (IOMM) for the system being tested.

(b) EL-15001, No. 2/GTD-3 EAX Peripheral Controller Circuit.

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(c) JD-XXXXXX-OCD, Office (Site) Configuration Drawing.

(d) Section 227-200-105, Processor Control and Display Console - Description and Use.

3. TEST OBJECTIVE

3.01 The objective of the test procedures in the section is to verify the allowed and denied status transitions of the CP and associated units by inputting messages via a maintenance terminal.

4. TEST PROCEDURES

4.01 In order to fully test the status transitions of the CP and associated units, it is necessary to determine the quantity of units equipped and the status of each. To determine this information, input on the terminal: DUMP STATUS CMC. The output will be a list of all (CMC) Control and Memory Complex units and their status.

4.02 For the CP, three copies (0, 1, and 2) are provided. Two copies each of the CM, RM, and clock are provided (0 and 1). The status should be "in service" (INS, INS.ACT or INS.SBY).

4.03 In the case of a unit listed as INS.SBY, copy 0 should be INS.ACT due to equipment dependency.

4.04 Sequentially perform the steps listed in Table 1 to test the CP status transitions; Table 2 to test the ~~SUS~~ status transitions; Table 3 to test the CM and RM status transitions; and Table 4 to test the clock status transitions.

4.05 Input all messages via a maintenance terminal.

4.06 If the operation for any step in the test procedure fails to produce the indicated results, correct the problem and perform the test on that unit again.

4.07 Each time the audible alarm sounds, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the chime and causes any SYSTEM ALARM lamp on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark.

Table 1. Control Processor Status Test Procedure.

STEP	OPERATION	RESULT
1	Input DUMP STATUS CP*	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP CP0 INS CP1 INS CP2 INS
2	Input PUT INS CP0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE CP0 INS TO INS
3	Input FORCE INS CP0	The results correspond to those in step 2.
4	Input PUT OOS CP0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the following lamps light: (a) MASTER STATUS CP1. (b) OOS CP0. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP0 INS TO OOS.MM MINOR ALARM

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Table 1. Control Processor Status Test Procedure (Continued).

STEP	OPERATION	RESULT
5	Input DIAG CP0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CP0 ATP STATUS CHANGE CP0 OOS.MM TO OOS.MM
6	Input PUT INS CP0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the following lamps go dark: (a) MASTER STATUS CP1. (b) OOS CP0. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CP0 ATP STATUS CHANGE CP0 OOS.MM TO INS
7	Input PUT ACT CP0	The terminal outputs ??IC044 INVALID PARAMETER AT CHAR 17, LINE 1
8	Input FORCE OOS CP0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the following lamps light:

Table 1. Control Processor Status Test Procedure (Continued).

STEP	OPERATION	RESULT
		(a) MASTER STATUS CP1. (b) OOS CP0. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP0 INS TO OOS.MM MINOR ALARM
9	Input FORCE INS CP0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the following lamps go dark: (a) MASTER STATUS CP1. (b) OOS CP0. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CP0 OOS.MM TO INS
10	Repeat steps 2 through 9, replacing CP0 with CP1.	The results correspond to those in steps 2 through 9, except CP0 is replaced by CP1.
11	Repeat steps 2 through 9, replacing CP0 with CP2.	The results correspond to those in steps 2 through 9, except CP0 is replaced by CP2.

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Table 2. Bus Status Test Procedure.

STEP	OPERATION	RESULT
1	Input DUMP STATUS BUS*	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP BUS0 INS BUS1 INS
2	Input PUT INS BUS0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE BUS0 INS TO INS
3	Input FORCE INS BUS0	The results correspond to those in step 2.
4	Input PUT OOS BUS0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the CM MIN lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE BUS0 INS TO OOS.MM MINOR ALARM

00295

Table 2. Bus Status Test Procedure (Continued).

STEP	OPERATION	RESULT
5	Input DIAG BUS0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS BUS0 ATP STATUS CHANGE OOS.MM TO OOS.MM
6	Input DIAG BUS1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC080 CONFIGURATION CONSTRAINT STATUS CHANGE BUS1 INS TO INS
7	Input PUT INS BUS0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the CM MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS BUS0 ATP STATUS CHANGE BUS0 OOS.MM TO INS
8	Input FORCE OOS BUS0	The results correspond to those in step 4.

00296

Table 2. Bus Status Test Procedure (Continued).

STEP	OPERATION	RESULT
9	Input FORCE INS BUS0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE BUS0 OOS.MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the CM MINOR lamp goes dark.
10	Repeat steps 2 through 9, replacing BUS0 with BUS1 and BUS1 with BUS0 (step 6).	The results correspond to those in steps 2 through 9, except BUS0 is replaced by BUS1, and in step 6, BUS1 is replaced by BUS0.

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Table 3. Command Matcher and Response Matcher States Test Procedure.

STEP	OPERATION	RESULT
1	Input DUMP STATUS CM*	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP CM0 INS CM1 INS
2	Input PUT OOS CM0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the CM MIN lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CM0 INS TO OOS.MM MINOR ALARM
3	Input DIAG CM0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CM0 ATP STATUS CHANGE OOS.MM TO OOS.MM
4	Input DIAG CM1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CM1 ATP STATUS CHANGE INS TO INS

00298

Table 3. Command Matcher and Response Matcher Status Test Procedure (Continued).

STEP	OPERATION	RESULT
5	Input FORCE OOS CM1	On the SAP, the following occur: (a) CMC EQUIPMENT MINOR lamp goes dark. (b) CMC EQUIPMENT MAJOR lamp lights. (c) SYSTEM ALARM MINOR lamp lights. On the PCDC, the following occur: (a) CM MIN lamp goes dark. (b) CM MAJ lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CM1 INS TO OOS.MM MAJOR ALARM
6	Input PUT INS CM1	On the SAP, the following occur: (a) CMC EQUIPMENT MINOR lamp lights. (b) CMC EQUIPMENT MAJOR lamp goes dark. (c) SYSTEM ALARM MINOR lamp lights. On the PCDC, the following occur: (a) CM MIN lamp lights. (b) CM MAJ lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CM1 ATP STATUS CHANGE CM1 OOS.MM TO INS

Table 3. Command Matcher and Response Matcher Status Test Procedure (Continued).

STEP	OPERATION	RESULT
7	Input FORCE INS CM0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CM0 OOS.MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the CM MIN lamp goes dark.
8	Repeat steps 1 through 7, replacing CM0 with RM0 and CM1 with RM1.	The results correspond to those in steps 1 through 7, except CM0 is replaced by RM0 and CM1 is replaced by RM1.

Table 4. Clock Status Test Procedure.

STEP	OPERATION	RESULT
1	Input DUMP STATUS PCLK*	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP PCLK0 INS.ACT PCLK1 INS.SBY
2	Input PUT INS PCLK0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PCLK0 INS.ACT TO INS.ACT
3	Input FORCE INS PCLK0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PCLK0 INS.ACT TO INS.ACT
4	Input DIAG PCLK0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PCLK0 INS.ACT TO INS.ACT

00301

Table 4. Clock Status Test Procedure (Continued).

STEP	OPERATION	RESULT
5	Input PUT OOS PCLK0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the CLOCK MIN lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PCLK0 INS.ACT TO OOS.MM MINOR ALARM R@XXXX JOB:XXXX STATUS CHANGE PCLK1 INS.SBY TO INS.ACT
6	Input DIAG PCLK0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PCLK0 ATP STATUS CHANGE PCLK0 OOS.MM TO OOS.MM
7	Input PUT INS PCLK0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the CLOCK MIN lamp goes dark.

00302

Table 4. Clock Status Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PCLK0 ATP STATUS CHANGE PCLK0 OOS.MM TO INS.SBY
8	Input PUT ACT PCLK0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PCLK0 ATP STATUS CHANGE PCLK0 INS.SBY TO INS. ACT R@XXXX JOB:XXXX STATUS CHANGE PCLK1 INS.ACT TO INS.SBY
9	Input FORCE OOS PCLK0	The results correspond to those in step 5.
10	Input FORCE ACT PCLK0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the CLOCK MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PCLK0 OOS.MM TO INS.ACT

00303

Table 4. Clock Status Test Procedure (Continued).

STEP	OPERATION	RESULT
		R@XXXX JOB:XXXX STATUS CHANGE PCLK1 INS.ACT TO INS.SBY
11	Input PUT OOS PCLK0	The results correspond to those in step 5.
12	Input PUT OOS PCLK1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC080 CONFIGURATION CONSTRAINT STATUS CHANGE PCLK1 INS.ACT TO INS.ACT
13	INPUT FORCE OOS PCLK1	The results correspond to those in step 12.
14	Input FORCE INS PCLK0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the CLOCK MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PCLK0 OOS.MM TO INS.SBY
15	Repeat steps 2 through 14, replacing PCLK0 with PCLK1, and in steps 12 and 13, PCLK1 with PCLK0.	The results correspond to those in step 2 through 14, except PCLK0 replaces PCLK1 and PCLK1 replaces PCLK0.

00304

TYPE 2B PROCESSOR COMPLEX
MEMORY UNIT AND MEMORY INTERFACE UNIT STATUS
INSTALLATION TEST PROCEDURES

CONTENTS

1. GENERAL

2. PREREQUISITES

3. TEST OBJECTIVE

4. TEST PROCEDURES

LIST OF TABLES

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Table 2. CMC Memory Units and Associated Test Procedures.

Table 3. MU Test Procedure.

Table 4. MIU Test Procedure.

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1. GENERAL

1.01 This section provides the procedure for testing the status, controls, and indications for the Memory Unit (MU) and Memory Interface Unit (MIU) of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisities, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the following conditions exist prior to performing the test in this section:

(a) All Type 2B Processor Complex units are free of faults and in service.

(b) The system configuration is in the full-duplex mode with all copies 0 primary.

(c) All lamps and pushbuttons on the Processor Control and Display Console (PCDC) are in their normal or unoperated position.

(d) All lamps on the Status and Alarm Panel (SAP) are unlit.

(e) One terminal is available for maintenance inputs.

(f) The System Monitor - Static and Dynamic Installation Test Procedure in Section 227-201-502 has been successfully completed.

(g) A level 2 initialization has been manually generated from the PCDC.

2.03 Test personnel should have access to the following documentation:

(a) The Input/Output Message Manual (IOMM) for the system being tested.

(b) EL-15003, No. 2/~~No. 3~~ GTD-3 EAX 64K x 33-Bit Store Circuit Drawing.

(c) EL-15004, No. 2/~~No. 3~~ EAX 128K x 33-Bit Store Circuit Drawing.

(d) JD-XXXXXOCD, Site Configuration Drawing.

(e) Section 227-200-105, Processor Control and Display Console - Description and Operation.

00306

3. TEST OBJECTIVE

3.01 The objective of the test procedures in this section is to verify the allowed and denied status transitions of the MU and MIU by inputting messages via a maintenance terminal.

4. TEST PROCEDURES

4.01 Determine all memory and memory interface units that are in service by following the procedure described in Table 1. The resulting list of equipped units may be checked against Table 2, which lists all memory and memory interface units that may be included in the Control and Memory Complex (CMC).

4.02 Because of equipment dependency, all units should be in service (INS, INS.SBY, or INS.ACT). In the case of an INS.SBY or INS.ACT unit, copy 0 should be INS.ACT at the onset of a test.

4.03 Sequentially perform the steps listed in Table 3 to test the MU status transitions, and in Table 4 to test the MIU status transitions.

4.04 Input all messages via a maintenance terminal.

4.05 If the operation for any step in the test procedure fails to produce the indicated results, correct the problem and perform the test on that unit again.

4.06 Each time the audible alarm sounds, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the alarm and causes any SYSTEM ALARM lamp on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark.

00367

Table 1. CMC Listing Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input DUMP STAT CMC	All equipped CMC units are listed and should be in service (INS, INS.ACT, or INS.SBY). In the case of an INS.SBY or INS.ACT hardware identifier, hardware copy 0 should be INS.ACT.

00368

Table 2. CMC Memory Units and Associated Test Procedures.

HARDWARE IDENTIFIER	ADDRESSES (COPY.INTERFACE UNIT.UNIT)	TEST PROCEDURE
MU	0.(0 to 3).(0 to 7) 1.(0 to 3).(0 to 7)	Table 3
MIU	0.(0 to 3) 1.(0 to 3)	Table 4

00309

Table 3. MU Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input DUMP STATUS MU*.*.* where * = all equipped members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP MU0.0.0 INS . . . MUa.a.a INS where a = last equipped member
2	Input PUT INS MU0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MU0.0.0 INS TO INS
3	Input FORCE INS MU0.0.0	The results are the same as those in step 2.
4	Input PUT OOS MU0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MU0.0.0 INS TO OOS MM MINOR ALARM On the SAP, the CMC EQUIPMENT MINOR and the SYSTEM ALARM MINOR lamps light. On the PCDC, the MEMORY MIN lamp lights.

Table 3. MU Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
5	Input DIAG MU0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MU0.0.0 ATP STATUS CHANGE MU0.0.0 OOS.MM TO OOS.MM
6	Input PUT INS MU0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MU0.0.0 ATP STATUS CHANGE MU0.0.0 OOS.MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the MEMORY MIN lamp goes dark.
7	Input FORCE OOS MU0.0.0	The results are the same as those in step 4.
8	Input FORCE INS MU0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MU0.0.0 OOS.MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the MEMORY MIN lamp goes dark.
9	Repeat steps 2 through 8 for each MU address outputted in step 1.	The results correspond to those in steps 2 through 8, except for appropriate changes in copy, address, and unit numbers.

Table 4. MIU Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input DUMP STATUS MIU*.* where * = all equipped members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP MIU0.0 INS . . . MIUa.a INS where a = last equipped member
2	Input PUT INS MIU0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MIU0.0 INS TO INS
3	Input FORCE INS MIU0.0	The results are the same as those in step 2.
4	Input PUT OOS MIU0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MIU0.0 INS TO OOS.MM MINOR ALARM On the SAP, the CMC EQUIPMENT MINOR and SYSTEM ALARM MINOR lamps light. On the PCDC, the MEMORY MIN lamp lights.

00312

Table 4. MIU Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
5	Input DIAG MIU0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MIU0.0 ATP STATUS CHANGE MIU0.0 OOS.MM TO OOS.MM
6	Input PUT INS MIU0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MIU0.0 ATP STATUS CHANGE MIU0.0 OOS MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the MEMORY MIN lamp goes dark.
7	Input FORCE OOS MIU0.0.0	The results are the same as those in step 4.
8	Input FORCE INS MIU0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MIU0.0.0 OOS.MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the MEMORY MIN lamp goes dark.
9	Repeat steps 2 through 8 for each address outputted in step 1.	The results correspond to those in steps 2 through 8, except for appropriate changes in copy and address numbers.

00313

TYPE 2B PROCESSOR COMPLEX
POWER ZONES STATUS
INSTALLATION TEST PROCEDURES

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00314

1. GENERAL

1.01 This section provides the installation test procedure for testing the status controls and indications for the power zones portion of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic No. 2 EAX, refer to Section 222-000-500; for an international No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the following conditions exist prior to performing the test procedures in this section:

(a) All Type 2B Processor Complex units are free of faults and in service.

(b) The system configuration is in the full-duplex mode with all copies 0 primary.

(c) All lamps and pushbuttons on the Processor Control and Display Console (PCDC) are in their normal or unoperated position.

(d) All lamps on the Status and Alarm Panel (SAP) are unlit.

(e) One terminal is available for maintenance inputs.

(f) Section 227-201-502, System Monitor Static and Dynamic Installation Test Procedure, has been successfully completed.

(g) A level 2 initialization has been manually generated from the PCDC.

2.03 Test personnel should have access to the following documentation:

(a) The Input/Output Message Manual (IOMM) for the system being tested.

(b) JD-XXXXX-OCD, Office (Site) Configuration Drawing.

(c) Section 227-200-105, Processor Control and Display Console Description and Operation.

(d) Power Zones Circuit Drawing.

00315

3. TEST OBJECTIVE

3.01 The objective of the test procedures in this section is to verify the allowed and denied status transitions of the power zone units.

4. TEST PROCEDURES

4.01 Determine the number of units in service as explained in paragraphs 4.02 and 4.03, and modify the test steps accordingly. Table 1 lists all units that may be included in these test procedures.

4.02 The number of equipped units must be available and listed using the procedure in Table 2, and may be checked against Table 1.

4.03 Because of equipment dependency, all units should be in service (INS, INS.SBY, or INS.ACT). In the case of an INS.SBY or INS.ACT unit, copy 0 should be INS.ACT at the onset of a test.

4.04 Sequentially perform the steps listed in Table 3, 4, and 5, to test the Central Processor Power Zone (CPPZ), Memory Power Zone (MPZ), and Peripheral Interface Power Zone (PIPZ) ~~CPPZ, MPZ, and PIPZ~~ status transitions, respectively.

4.05 If the operation for any step in the test procedure fails to produce the indicated result/system response, correct the problem and perform the test on that unit again.

4.06 Input all messages via a maintenance terminal.

4.07 Whenever an audible alarm sounds, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the alarm and causes the appropriate SYSTEM ALARM lamps on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark. Any PERIPHERAL ALARMS lamps that may have lit, will remain lit, until the problem is corrected. If any subsequent system alarms should occur, the appropriate audible alarm will sound again and lamp(s) will light.

00316

Table 1. Hardware Identifiers, Addresses, and Test Procedures.

HARDWARE IDENTIFIER	ADDRESSES			TEST PROCEDURE
	COPY	INTERFACE	UNITS	
CPPZ	0			Table 3
	1			
	2			
MPZ	0	0 to 3	0 and 1	Table 4
	1	0 to 3	0 and 1	
PIPZ	0		0 and 1	Table 5
	1		0 and 1	

00317

Table 2. Procedure for Obtaining List of Equipped Units.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input DUMP STATUS CMC	All equipped CMC units in service are listed as INS, INS.ACT, or INS.SBY. In the case of an INS.SBY or INS.ACT unit, hardware copy ∅ should be INS.ACT.

00318

Table 3. CPPZ Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input DUMP STATUS CPPZ* where * = all members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP CPPZ0 INS CPPZ1 INS CPPZ2 INS
2	Input PUT INS CPPZ0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID TRANSITION STATUS CHANGE CPPZ0 INS TO INS
3	Input FORCE INS CPPZ0	The results correspond to those of step 2.
4	Input PUT OOS CPPZ0	On the PCDC, the OOS CP0 and MASTER STATUS CP1 lamps light. On the SAP, the CMC EQUIPMENT MINOR and SYSTEM ALARM MINOR lamps light. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CPPZ0 INS TO OOS.MM MINOR ALARM

00319

Table 3. CPPZ Test Procedure (Continued).

STEP	OPERATION	RESULT/ SYSTEM RESPONSE
5	Input PUT INS CPPZØ	On PCDC and SAP, all lamps that lit in step 4 go dark. The terminal outputs OK JOB:XXXX RØXXXX JOB:XXXX STATUS CHANGE CPPZØ OOS.MM TO INS
6	Input FORCE OOS CPPZØ	The results correspond to those in step 4.
7	Input PUT INS CPPZ1	The results correspond to those in step 5.
8	Repeat steps 2 through 7, replacing CPPZØ with CPPZ1.	The results correspond to those in steps 2 through 7, except CPPZ1 replaces CPPZØ, CP1 replaces CPØ, and CP2 replaces CP1.
9	Repeat steps 2 through 7, replacing CPPZØ with CPPZ2.	The results correspond to those in steps 2 through 7, except CPPZ2 replaces CPPZØ, CP2 replaces CPØ, and CPØ replaces CP1.

Table 4. MPZ Test Procedure.

STEP	OPERATION	RESULT / SYSTEM RESPONSE
1	Input DUMP STATUS MPZ*.*.* where * = all members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP MPZ0.0.0 INS MPZ0.1.0 INS MPZ0.3.1 INS MPZ1.0.0 INS MPZ1.3.1 INS (depending on the number of equipped MPZ's)
2	Input PUT INS MPZ0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MPZ0.0.0 INS TO INS
3	Input FORCE INS MPZ0.0.0	The results correspond to those in step 2.
4	Input PUT OOS MPZ0.0.0	On the SAP, the CMC EQUIPMENT MINOR AND SYSTEM ALARM MINOR lamps light. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MPZ0.0.0 INS TO OOS.MM

00321

Table 4. MPZ Test Procedure (Continued).

STEP	OPERATION	RESULT/ SYSTEM RESPONSE
5	Input PUT INS MPZ∅.∅.∅	The CMC EQUIPMENT MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MPZ∅.∅.∅ OOS.MM TO INS
6	Input FORCE OOS MPZ∅.∅.∅	The results correspond to those in step 4.
7	Input FORCE INS MPZ∅.∅.∅	The results correspond to those in step 5.
8	Repeat steps 2 through 7, replacing MPZ∅.∅.∅ with the subsequent MPZ's in the order shown in the RESULT column of step 1.	The results correspond to those in steps 2 through 7, with the MPZ number changed as appropriate.
	result/system response	

00322

Table 5. PIPZ Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input DUMP STATUS PIPZ*.* where * = all members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP PIPZØ.Ø INS PIPZØ.1 INS PIPZ1.Ø INS PIPZ1.1 INS
2	Input PUT INS PIPZØ.Ø	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TCØ76 INVALID STATUS TRANSITION STATUS CHANGE PIPZØ.Ø INS TO INS
3	Input FORCE INS PIPZØ.Ø	The results correspond to the results in step 2.
4	Input PUT OOS PIPZØ.Ø	On the SAP, the CMC EQUIPMENT MINOR and SYSTEM ALARM MINOR lamps light. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PIPZØ.Ø INS TO OOS.MM

00323

Table 5. PIPZ Test Procedure (Continued).

STEP	OPERATION	RESULT / SYSTEM RESPONSE
5	Input PUT INS PIPZ∅.∅	The CMC EQUIPMENT MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PIPZ∅.∅ OOS.MM TO INS
6	Input FORCE OOS PIPZ∅.∅	The results correspond to those in step 4.
7	Input FORCE INS PIPZ∅.∅	The results correspond to those in step 5.
8	Input PUT INS PIPZ∅.1	The results correspond to those in step 2, except PIPZ∅.∅ is replaced by PIPZ∅.1.
9	Input FORCE INS PIPZ∅.1	The results correspond to those in step 3, except PIPZ∅.∅ is replaced by PIPZ∅.1.
10	Input PUT OOS PIPZ∅.1	On the SAP, the CMC EQUIPMENT MINOR and SYSTEM ALARM MINOR lamps light. OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PIPZ∅.1 INS TO OOS.MM

00324

Table 5. PIPZ Test Procedure (Continued).

STEP	OPERATION	RESULT / SYSTEM RESPONSE
11	Input PUT INS PIPZ0.1	The CMC EQUIPMENT MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PIPZ0.1 OOS.MM TO INS
12	Input FORCE OOS PIPZ0.1	The results correspond to those in step 10.
13	Input FORCE INS PIPZ0.1	The results correspond to those in step 11.
14	Repeat steps 2 through 13, replacing PIPZ0.0 with PIPZ1.1 and PIPZ0.1 with PIPZ1.0.	The results correspond to those in steps 2 through 13, except PIPZ1.1 replaces PIPZ0.0 and PIPZ1.0 replaces PIPZ0.1.

TYPE 2B PROCESSOR COMPLEX PERIPHERAL CONTROLLER AND PERIPHERAL CONTROLLER INTERFACE UNIT STATUS INSTALLATION TEST PROCEDURES

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00326

1. GENERAL

1.01 This section provides the installation test procedure for testing the status, controls, and indications for the Peripheral Controller (PC) and Peripheral Controller Interface Unit (PIU) portion of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the Field Implementation Plan for the system being installed (i.e., for a domestic No. 2 EAX, refer to Section 222-000-500; for an international No. 2 EAX, refer to Section 229-000-501IT.

2.02 Ensure that the following conditions exist prior to performing the test procedures in this section:

(a) All Type 2B Processor Complex units are free of faults and in service.

(b) The system configuration is in the full-duplex mode with all copies 0 primary.

(c) All switches and pushbuttons on the Processor Control and Display Console (PCDC) are in their normal or unoperated position.

(d) All lamps on the SYSTEM STATUS AND ALARM subpanel of the Status and Alarm Panel (SAP) are unlit.

(e) One terminal is available for maintenance inputs.

(f) Section 227-201-502, System Monitor - Static and Dynamic Installation Test Procedure, has been successfully completed.

(g) A level 2 initialization has been manually generated from the PCDC.

2.03 Test personnel should have access to the following documentation:

(a) The Input/Output Message Manual (IOMM) for the system being tested.

(b) EL-15001, No. 2 EAX/GTD-3 EAX Peripheral Controller Circuit.

(c) JD-XXXXXX-OCD, Office (Site) Configuration Drawing.

00327

(d) Section 227-200-105, Processor Control and Display Console - Description and Operation.

3. TEST OBJECTIVE

3.01 The objective of the test procedures in this section is to verify the allowed and denied status transitions for PC units and PIU's by inputting messages via a maintenance terminal.

4. TEST PROCEDURES

4.01 In order to fully test the status transitions of the PC units and PIU's, it is necessary to determine the quantity of PC units equipped and the status of each PC unit and PIU. To determine this information, input the following via terminal: DUMP STATUS CMC. The terminal will output a list of all CMC units and their status.

4.02 For the PC, two copies (0 and 1) are provided, and each copy can have up to 32 units (0 through 31). Two copies of the PIU are provided (0 and 1). The status should be in service (INS, INS.ACT, or INS.SBY).

4.03 In the case of a unit listed as INS.SBY, copy 0 should be INS.ACT due to equipment dependency.

4.04 Sequentially perform the steps listed in Tables 1 and 2 to test the PC and PIU status transitions.

4.05 Input all messages via a maintenance terminal.

4.06 If the operation for any step in either test procedure fails to produce the indicated result/system response, correct the problem and perform the test on that unit again.

00328

4.07 Each time the audible alarm sounds during testing, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the audible alarm and causes the appropriate SYSTEM ALARM lamp(s) on the SAP to go dark. Any PERIPHERAL ALARMS lamps that may have lit, will remain lit until the problem is corrected. If any subsequent system alarms should occur, the appropriate audible alarm will sound again and lamp(s) will light.

00329

Table 1. Peripheral Controller Status Test Procedure.

STEP	OPERATION	RESULT
1	Input DUMP STATUS PC*.* where * = all members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP PC0.0 INS.ACT PC0.1 INS.ACT . . . PC0.a INS.ACT PC1.0 INS.SBY PC1.1 INS.SBY . . . PC1.a INS.SBY where a = last equipped member
2	Input PUT INS PC0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PC0.0 INS.ACT TO INS.ACT
3	Input FORCE INS PC0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PC0.0 INS.ACT TO INS.ACT

Table 1. Peripheral Controller Status Test Procedure (Continued).

STEP	OPERATION	RESULT
4	Input PUT OOS PC0.0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the PERIPHERAL MIN lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PC0.0 INS.ACT TO OOS.MM MINOR ALARM JOB:XXXX STATUS CHANGE PC1.0 INS.SBY TO INS.ACT
5	Input PUT ACT PC0.0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the PERIPHERAL MIN lamp goes dark. The terminal outputs OK JOB:XXXX DIAG RESULTS PC0.0 ATP STATUS CHANGE PC0.0 OOS.MM TO INS.ACT XXXX JOB: ~~YYYY (YYYY = XXXX + 1)~~ STATUS CHANGE PC0.1 INS.ACT TO INS.SBY

00331

Table 1. Peripheral Controller Status Test Procedure (Continued).

STEP	OPERATION	RESULT
6	Input PUT OOS PC0.0	The results correspond to those in step 4.
7	Input FORCE ACT PC0.0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the PERIPHERAL MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PC0.0 OOS.MM TO INS.ACT JOB:XXXX STATUS CHANGE PC1.0 INS.ACT INS.SBY
8	Input PUT OOS PC0.0	The results correspond to those in step 4.
9	Input PUT INS.PC0.0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the PERIPHERAL MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PC0.0 ATP STATUS CHANGE PC0.0 OOS.MM TO INS.SBY

00332

Table 1. Peripheral Controller Status Test Procedure (Continued).

STEP	OPERATION	RESULT
10	Input FORCE OOS PC0.0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, THE PERIPHERAL MIN lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PC0.0 INS.SBY TO OOS.MM MINOR ALARM
11	Input FORCE INS.PC0.0	On the SAP, CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the PERIPHERAL MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PC0.0 OOS.MM TO INS.SBY
12	Input FORCE INS PC0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PC0.0 STF 0000 0000 STATUS CHANGE PC0.0 INS.SBY TO INS.ACT JOB:XXXX STATUS CHANGE PC1.0 INS.ACT TO INS.SBY

00333

Table 1. Peripheral Controller Status Test Procedure (Continued).

STEP	OPERATION	RESULT
13	Input PUT OOS PC0.0	The results correspond to those in step 4.
14	Input FORCE INS.PC0.0	The results correspond to those in step 9.
15	Input FORCE ACT PC0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PC0.0 INS.SBY TO INS.ACT JOB:XXXX STATUS CHANGE PC1.0 INS.ACT TO INS.SBY
16	Input DIAG PC0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PC0.0 INS.ACT TO INS.ACT
17	Input PUT OOS PC0.0	The results correspond to those in step 4.
18	Input DIAG PC0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PC0.0 ATP STATUS CHANGE PC0.0 OOS.MM TO OOS.MM

00334

Table 1. Peripheral Controller Status Test Procedure (Continued).

STEP	OPERATION	RESULT
19	Input FORCE INS.PC0.0	The results correspond to those in step 9.
20	Repeat steps 2 through 19, replacing PC0.0 with PC1.0.	The results correspond to those in steps 2 through 19, except PC0.0 replaces PC1.0 and PC1.0 replaces PC0.0.
21	Repeat steps 2 through 20 for all equipped units.	The results correspond to those in steps 2 through 20, except the second number of the address (unit number) corresponds to the unit number entered on the terminals.

00335

Table 2. Peripheral Controller Interface Unit Status Test Procedure.

STEP	OPERATION	RESULT
1	Input DUMP STATUS PIU* where * = all equipped members	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP PIU0 INS PIU1 INS
2	Input PUT INS PIU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE PIU0 INS TO INS
3	Input FORCE INS PIU0	The results correspond to those in step 2.
4	Input PUT OCS PIU0.0	On the SAP, the following lamps light: (a) CMC EQUIPMENT MINOR. (b) SYSTEM ALARM MINOR. On the PCDC, the PERIPHERAL MIN lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PIU0 INS TO OOS.MM MINOR ALARM

00336

Table 2. Peripheral Controller Interface Unit Status Test Procedure (Continued).

STEP	OPERATION	RESULT
5	Input DIAG PIU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PIU0 ATP STATUS CHANGE PIU0 OOS.MM TO OOS.MM
6	Input DIAG PIU1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX CONSTRAINT TC080 CONFIGURATION ~~CONTRAINT~~ STATUS CHANGE PIU1 INS TO INS
7	Input PUT INS PIU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PIU0 ATP STATUS CHANGE PIU0 OOS.MM TO INS On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the PERIPHERAL MIN lamp goes dark.
8	Input FORCE OOS PIU0	The results correspond to those in step 4.

00337

Table 2. Peripheral Controller Interface Unit Status Test Procedure (Continued).

STEP	OPERATION	RESULT
9	Input PUT OOS PIU1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC080 CONFIGURATION CONSTRAINT STATUS CHANGE PIU1 INS TO INS
10	Input FORCE OOS PIU1	The results correspond to those in step 9.
11	Input FORCE INS PIU0	On the SAP, the CMC EQUIPMENT MINOR lamp goes dark. On the PCDC, the PERIPHERAL MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE PIU0 OOS.MM TO INS
12	Repeat steps 2 through 11, replacing PIU0 with PIU1 and, in steps 6,9, and 10, replacing PIU1 with PIU0.	The results correspond to those in steps 2 through 11, except PIU0 replaces PIU1 and, in steps 6,9, and 10, PIU1 replaces PIU0.

00338

TYPE 2B PROCESSOR COMPLEX
TERMINAL STATUS
INSTALLATION TEST PROCEDURE

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Figure 1. Typical Terminal c.d Output Message.

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00339

1. GENERAL

1.01 This section provides the procedure for testing the status, diagnostic, and configuration controls for terminals of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed. For example, for a No. 2 EAX, [redacted] refer to Section 222-000-500.

2.02 Ensure that the following conditions exist prior to performing the test procedure in this section:

(a) All lamps and pushbuttons on the Processor Control and Display Console (PCDC) are in their normal or unoperated positions, and all lamps in the SYSTEM STATUS AND ALARM subpanel of the Status and Alarm Panel (SAP) are unlit.

(b) Two terminals are available.

NOTE: Designate one terminal as terminal a.b and the other as terminal c.d

where

a and c = the Input/Output Access Frame (IOAF) numbers

b and d = the terminal channel numbers

(c) The installation test procedure for the IOAF in Section 227-203-510 has been successfully completed.

2.03 Test personnel should have access to the following:

(a) An Input/Output Message Manual (IOMM) for the system being tested.

(b) JD-XXXXX-OCD, Office (Site) Configuration Drawing.

(c) The terminal manufacturer's manual.

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3. TEST OBJECTIVE

3.01 The objective of this test procedure is to verify the allowed and denied status transitions of the terminals.

4. TEST PROCEDURE

4.01 Sequentially perform the steps in Table 1 to test terminal status transitions. Input all messages via terminal a.b. Refer to Figure 1 for a typical terminal c.d output message.

4.02 If any step in this test procedure fails to produce the indicated result/system response, correct the problem and perform the entire procedure again.

4.03 Whenever testing causes an audible alarm to sound, depress the AUDIBLE ALARM RESET pushbutton on the SAP . This action silences the alarm and causes the appropriate SYSTEM ALARM lamp on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark. Any PERIPHERAL ALARMS lamps will remain lit, and any subsequent system alarms (if any) will cause the appropriate alarm to sound and lamp(s) to light.

00341

Table 1. Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
	NOTE: All lamps are located on the SAP.	
1	Input PUT OOS TERM c.d	The PERIPHERAL EQUIPMENT MINOR lamp lights. The I/O TERMINAL MINOR lamp lights. Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE TERM c.d INS.IDLE TO OOS.MM MINOR ALARM
2	Input PUT INS TERM c.d	The PERIPHERAL EQUIPMENT MINOR lamp goes dark. The I/O TERMINAL MINOR lamp goes dark. Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS TERM c.d ATP STATUS CHANGE TERM c.d OOS.MM TO INS.IDLE Terminal c.d outputs a typical message (Figure 1).
3	Input DIAG TERM c.d	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS TERM c.d ATP STATUS CHANGE TERM c.d INS.IDLE TO INS.IDLE Terminal c.d outputs a typical message (Figure 1).
4	Input FORCE OOS TERM c.d	The PERIPHERAL EQUIPMENT MINOR lamp lights. The I/O TERMINAL MINOR lamp lights.

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
		Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE TERM c.d INS.IDLE TO OOS.MM MINOR ALARM
5	Input DIAG TERM c.d	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS TERM c.d ATP STATUS CHANGE TERM c.d OOS.MM TO OOS.MM
6	Input PUT INS TERM c.d	The PERIPHERAL EQUIPMENT MINOR lamp goes dark. The I/O TERMINAL MINOR lamp goes dark. Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS TERM c.d ATP STATUS CHANGE TERM c.d OOS.MM TO INS.IDLE Terminal c.d outputs a typical message (Figure 1).
7	Input FORCE INS TERM c.d	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX TCØ76 INVALID STATUS TRANSITION STATUS CHANGE TERM c.d INS.IDLE TO INS.IDLE
8	Input PUT OOS TERM c.d	The PERIPHERAL EQUIPMENT MINOR lamp lights. The I/O TERMINAL MINOR lamp lights. Terminal a.b outputs

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
		OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE TERM^c.d INS.IDLE TO OOS.MM MINOR ALARM
9	Input PUT OOS TERM^a,b	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX TC073 OOS LIMIT EXCEEDED STATUS CHANGE TERM^a.b INS.IDLE TO INS.IDLE
10	Input FORCE OOS TERM^a.b	The PERIPHERAL EQUIPMENT MAJOR lamp lights. The I/O TERMINAL MAJOR lamp lights.
11	Input FORCE INS TERM^a.b	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE TERM^a.b OOS.MM TO INS.IDLE The PERIPHERAL EQUIPMENT MAJOR lamp goes dark. The I/O TERMINAL MAJOR lamp goes dark.
12	Input PUT INS TERM^c.d	The PERIPHERAL EQUIPMENT MINOR lamp goes dark. The I/O TERMINAL MINOR lamp goes dark. Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS TERM^c.d ATP STATUS CHANGE TERM^c.d OOS.MM TO INS.IDLE Terminal c.d outputs a typical message (Figure 1).

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
13	Input FORCE INS TERM c.d	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX TC073 INVALID STATUS TRANSITION STATUS CHANGE TERM c.d INS.IDLE TO INS.IDLE
14	Input ROUT TERM	Terminal a.b outputs OK JOB:XXXX R@XXXX JOB:XXXX ROUTINE TERM DONE Terminal c.d and any other terminals in the office output a typical message (Figure 1).

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```
TERM_TEST: ABCDEFGHIJKLMNOPQRSTUVWXYZ "#$%&'()*+,-./:;<=>?@[ ] 0123456789
TERM_TEST: ABCDEFGHIJKLMNOPQRSTUVWXYZ "#$%&'()*+,-./:;<=>?@[ ] 0123456789
TERM_TEST: ABCDEFGHIJKLMNOPQRSTUVWXYZ "#$%&'()*+,-./:;<=>?@[ ] 0123456789

AFTER EACH LINE, BELL RINGS.
```

Figure 1. Typical Terminal c.d Output Message.

TYPE 2B PROCESSOR COMPLEX
PROCESSOR CONTROL AND DISPLAY CONSOLE
CONTROLS AND FUNCTIONS
INSTALLATION TEST PROCEDURE

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SECTION 227-205-501
ISSUE 1

1. GENERAL

1.01 This section provides the installation test procedure for testing the features of the Type 2B Processor Control and Display Console (PCDC).

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the following conditions exist before performing the test procedure in this section:

(a) All Control and Memory Complex (CMC) units are free of fault and are in service.

(b) The system configuration is in a maximum configuration as follows:

 (1) All three Central Processors (CP's) (i.e., CP0, CP1, and CP2) are active.

 (2) Both buses (i.e., BUS0 and BUS1) are active.

 (3) Both Peripheral Interface Units (PIU's) (i.e., PIU0 and PIU1) are active.

 (4) All copies of memory are in service and active.

(c) One terminal is available for system messages.

(d) The Status and Alarm Panel (SAP) is available.

(e) All X-ray test procedures have been successfully completed.

3. TEST OBJECTIVE

3.01 The objective of the test procedure in this section is to verify the operation of the PCDC features.

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4. TEST PROCEDURE

4.01 Sequentially perform the steps listed in Table 1, executing the operation described and verifying that the expected result occurs.

4.02 All input and output is on the PCDC unless specifically specified as otherwise.

4.03 If the operation for any step fails to produce the indicated results, correct the problem and perform the step again.

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Table 1. Test Procedure.

STEP	OPERATION	RESULT
1	Depress and hold the FUNCTIONS LAMP TEST pushbutton.	All lamps light, except the FUNCTIONS LAMP TEST and CLEAR lamps. Upon release of the pushbutton, the lamps return to their original state.
2	Depress and release the ENTRY START pushbutton.	The ENTRY START lamp lights and the display clears.
3	Depress and release the CLEAR pushbutton.	The ENTRY START lamp goes dark and the display returns to its original state.
4	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits 11. (c) Depress the FUNCTIONS DATA FCN pushbutton.	The following is displayed: *ABCDEFGHIJKLMNOPQRSTUVWXYZ[]{}
5	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits 12. (c) Depress the FUNCTIONS DATA FCN pushbutton.	The following is displayed: 0123456789@>=< ;/.!="#$%&(')+,:

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
6	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits 13. (c) Depress the FUNCTIONS DATA FCN pushbutton.	The status of the lamps is as follows: LAMP — STATUS CE MAJ — On MONITOR FIRM RCVR — Unchanged MONITOR SOFT RCVR — Unchanged MONITOR RELOAD — Unchanged MONITOR SIA — Off INIT — On FUNCTIONS MCS — Off FUNCTIONS DATA FCN — On CLOCK MIN — On CE MIN — Off DMA MAJ — On DMA MIN — Off PERIF MAJ — On PERIF MIN — Off MEMORY MAJ — On MEMORY MIN — Off
7	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits 14. (c) Depress the FUNCTIONS DATA FCN pushbutton.	The status of the lamps is as follows: LAMP — STATUS CE MAJ — Off MONITOR FIRM RCVR — Unchanged MONITOR SOFT RCVR — Unchanged MONITOR RELOAD — Unchanged MONITOR SIA — On INIT — Off FUNCTIONS MCS — On FUNCTIONS DATA FCN — Off CLOCK MIN — Off CE MIN — On DMA MAJ — Off DMA MIN — On PERIF MAJ — Off PERIF MIN — On MEMORY MAJ — Off MEMORY MIN — On

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
8	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits 15. (c) Depress the FUNCTIONS DATA FCN pushbutton.	The status of the lamps restores to the state prior to performing step 6.
9	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits FFFFFFFF. (c) On the SYSTEM STATUS AND ALARM subpanel of the SAP, depress the MESSAGE CLASS(S) SUPPRESSED pushbutton.	On the SYSTEM STATUS AND ALARM subpanel of the SAP, the MESSAGE CLASS(S) SUPPRESSED lamp lights.
10	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter digits 00000000. (c) On the SYSTEM STATUS AND ALARM subpanel of the SAP, depress the MESSAGE CLASS(S) SUPPRESSED pushbutton.	On the SYSTEM STATUS AND ALARM subpanel of the SAP, the MESSAGE CLASS(S) SUPPRESSED lamp goes dark.

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Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
11	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter the characters 22E1. (c) Simultaneously depress the FORCE XCUTE and OOS CP0 pushbuttons.	The MONITOR RELOAD and INIT lamps momentarily light. The FORCE XCUTE and the OOS CP0, CP1, and CP2 lamps light. The terminal outputs S@XXXX SIA LEVEL 1 INITIALIZATION COMPLETED FORCE IN EFFECT
12	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter the characters 22E1. (c) Simultaneously depress the FORCE XCUTE and OOS CP1 pushbuttons.	The MONITOR RELOAD and INIT lamps momentarily light. The FORCE XCUTE and the OOS CP0, CP1, and CP2 lamps light. The terminal output is the same as in step 11.
13	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter the characters 22E1. (c) Simultaneously depress the FORCE XCUTE and OOS CP2 pushbuttons.	The MONITOR RELOAD and INIT lamps momentarily light. The FORCE XCUTE and the OOS CP0, CP1, and CP2 lamps light. The terminal output is the same as in step 11.

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Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
14	Perform the following: (a) Depress the ENTRY START pushbutton. (b) Simultaneously depress the FORCE XCUTE and OOS CP2 pushbuttons.	The FORCE XCUTE lamp goes dark.
15	Perform the following: (a) Depress the ENTRY START pushbutton. (b) At the keypad, enter the digit 1. (c) Simultaneously depress the FORCE XCUTE and INIT pushbuttons.	The INIT lamp momentarily lights. All lamps go dark and the terminal outputs S@XXXX SIA LEVEL 1 INITIALIZATION COMPLETED

TYPE 2B PROCESSOR COMPLEX
TERMINAL OPTION FEATURES
INSTALLATION TEST PROCEDURE

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Figure 8. Sample Option 8 Printout.

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1. GENERAL

1.01 This section provides the installation test procedure for testing the terminal option features of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic version No. 2 EAX, refer to Section 222-000-500; for an international version No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the following conditions exist before performing the test procedure in this section:

(a) All Type 2B Processor Complex units are free of known faults and are capable of being placed into service.

(b) All lamps on the Status and Alarm Panel (SAP) of the Maintenance Status and Alarm Frame (MSAF) are unlit.

(c) All equipped terminals are available for maintenance inputs and are functioning properly. The minimum requirement is two terminals, Control Maintenance Terminal One (CMT1) and a remote/alternate terminal (CMT2).

(d) A level 2 initialization has been manually generated from the Processor Control and Display Console (PCDC).

(e) Section 227-203-507, Terminal Status Installation Test Procedure, has been successfully completed.

2.03 Test personnel should have access to the following documentation:

(a) An Input/Output Message Manual (IOMM) for the system being tested.

(b) A Repair Manual (RM) for the system being tested.

(c) A Recent Change (RC) user's manual for the system being tested.

(d) JD-XXXXX-OCD, Office (Site) Configuration Drawing.

3. TEST OBJECTIVE

3.01 The objective of the test procedure in this section is to verify message class routing and other terminal option features.

4. TEST PROCEDURE

4.01 Sequentially perform the steps listed in Table 1 to verify the terminal option features. Tables 2 through 7 list the various messages, mnemonics, and codes to be used in Table 1.

4.02 Figures 1 through 8 show various sample terminal printouts used in Table 1.

4.03 Input all messages via a maintenance terminal. If no specific terminal is defined, CMT1 is to be used.

4.04 If the operation for any step in the test procedure fails to produce the indicated results, correct the problem and perform that step again.

4.05 Each time the audible alarm sounds, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the alarm and causes any SYSTEM ALARM lamp on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark.

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Table 1. Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Using the recent change messages (steps 1 through 6 in Table 2), change the Routing Type (RT) for Output Message Class (OMC) 11 from the engineered data base value to RTO. NOTES: 1. Refer to Table 3 for the OMC mnemonics. 2. Refer to Table 5 for the RT codes.	The results are listed in Table 2, steps 1 through 6. NOTE: Record the old data from recent change for re-use in steps 19 of this test procedure.
2	Input PUT OOS LINE 0.0.0.0.0.0	On the SAP, the LINE CKTS MINOR lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE LINE 0.0.0.0.0.0 INS TO OOS.MM
3	Input PUT OOS CMT1	On the SAP, the I/O TERMINAL MINOR lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT1 INS TO OOS.MM
4	Input PUT INS LINE 0.0.0.0.0.0	On the SAP, the LINE CKTS MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE LINE 0.0.0.0.0.0 OOS.MM TO INS

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Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
5	Input PUT INS CMT1	On the SAP, the I/O TERMINAL MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT1 OOS.MM TO INS
6	Input DUMP STATUS LINE 0.0.0 0.0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS DUMP LINE 0.0.0.0.0.0.0 INS IDLE
7	Using recent-change messages in Table 2 (steps 1 through 6), change the RT for OMC 11 from RT0 to RT1. NOTE: Refer to Table 5 for the required amounts of terminals for each RT.	The results are listed in Table 2, steps 1 through 6.
8	Input PUT OOS LINE 0.0.0.0.0. 0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE LINE 0.0.0.0.0.0.0 INS TO INS.MM
9	Input PUT OOS (CMT1)	CMT2 outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT1 INS TO OOS.MM

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Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
10	Input PUT INS LINE 0.0.0.0 0.0.0	CMT2 outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE LINE 0.0.0.0.0.0.0 OOS.MM TO INS
11	Input PUT INS CMT1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT1 OOS.MM TO INS
12	Repeat steps 7 through 11 for RT codes 2, 3, and 5. These RT's require that two terminals be specified. If more than two terminals exist in the office, vary the CMT1 and the CMT2 for the different RT codes.	The results correspond to the results in steps 7 through 11.
13	Using the recent-change messages in Table 2 (steps 1 through 6), change the RT code of OMC 11 to RT4. RT4 requires that three terminals be specified, if possible. If only two terminals exist, designate the second terminal CMT2.	The results are listed in Table 2, steps 1 through 6.
14	Input PUT OOS LINE 0.0.0.0 0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE LINE 0.0.0.0.0.0.0 INS TO OOS.MM

00361

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
15	Input PUT OOS CMT1	CMT2 outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT1 INS TO OOS.MM
16	Input PUT OOS CMT2 NOTE: Perform this step only if the alternate and remote terminals are not the same.	The specified remote terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT2 INS TO OOS.MM
17	Input PUT INS LINE 0.0.0.0 0.0.0	The specified remote terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE LINE 0.0.0.0.0.0.0 OOS.MM TO INS
18	Input (a) PUT INS CMT1 (b) PUT INS CMT2	The terminal outputs (a) OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT1 OOS.MM TO INS (b) OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE CMT2 OOS.MM TO INS

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
19	Using the recent-change messages in Table 2 (steps 1 through 6), change OMC 11 to the engineered data base value. NOTE: The data base value can be obtained from the old data in step 1.	The OMC 11 new data is placed into memory for the proper RT.
20	Input DIAG LINE 0.0.0.0.0.0.0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS LINE 0.0.0.0.0.0.0 DN ATTACHED XXX-XXXX ATP STATUS CHANGE LINE 0.0.0.0.0.0.0 INS.IDLE TO INS.IDLE
21	Using a daisy chain, strap pin 65 of the Line Control Circuit Frame (LCCF) 000 card, slot B-01, to ground.	
22	Input DIAG LINE 0.0.0.0.0.0.0	The results correspond to the results in Figure 1.
23	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 2	The results correspond to the results in Figure 2.

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Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
24	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 3	The results correspond to the results in Figure 3.
25	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 4	The results correspond to the results in Figure 4.
26	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 5	The results correspond to the results in Figure 5.
27	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 5 ITER 3	The results correspond to the results in Figure 6.
28	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 6	The results correspond to the results in Figure 7.
29	Input DIAG LINE 0.0.0.0.0.0.0 PRINT 8	The results correspond to the results in Figure 8.
30	Remove the ground strap applied to pin 65 in step 21.	

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Table 2. Recent-Change Input/Output Messages.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input ALLOW RC	The terminal outputs OK DONE
2	Input BEGIN RC MODIFY MODE	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX SWITCH TO OLD BUS CONFIRMED RC READY NOTE: The SWITCH TO OLD BUS CONFIRMED portion of the message may not be outputted.
3	Input CHANGE OMC LDIA RTO CMT1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX ADDRESS OLD DATA NEW DATA aaaaa b cdddddd bcdddddd NEW DATA LOADED IN COPY 1 PS RC READY where a = Process Store (PS) address b = routing type c = not used d = terminal functions (refer to Table 4)
4	Input PUT RC ONLINE	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX SWITCH TO NEW BUS CONFIRMED RC READY

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Table 2. Recent-Change Input/Output Messages (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
5	Input PUT RC DUPLEX	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX NEW DATA LOADED IN COPY 0 PS SWITCH TO OLD BUS CONFIRMED RC READY NOTE: All PS 0 units are diagnosed and put in service.
6	Input END RC BATCH	The terminal outputs OK RC ENDED
7	Repeat steps 1 through 6 for all RT changes 0 through 5, varying the terminal in step 3 when required.	The results correspond to the results in steps 1 through 6.

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Table 3. Output Message Class Mnemonics.

OMC NUMBER	MNEMONIC	OMC DESCRIPTION
0	Not Used	
1	CRCV	Common Recovery Messages
2	PRCV	Peripheral Recovery Messages
3	SYSA	System Alarm Messages
4	CCHG	Call Charging Messages
5	ANNC	Annoyance Call Messages
6	STCN	Stuck Coin Messages
7	LPRM	Line Permanent Messages
8	CDIA	Common Diagnostic Messages
9	PDIA	Peripheral Diagnostic Messages
10	TDIA	Trunk Diagnostic Messages
11	LDIA	Line Diagnostic Messages
12	NSMM	Network Switch Management Peg Count Messages
13	NSMO	Network Switch Management Overload Indicator Report
14	NSMI	Network Switch management Ineffective Message Attempts
15	NSMT	Network Switch Management Trunk Group Reports
16	TDAD	Traffic Data Administration (TDA) Display Messages
17	TDAC	TDA Control Messages
18	TDAS	TDA Summary Reports, CCS Ticket Studies, Wake Up Denied Messages
19	SMSU	System Malfunction Analysis (SMA) Summary Reports
20	SMAP	SMA Periodic Reports

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Table 3. Output Message Class Mnemonics.

OMC NUMBER	MNEMONIC	OMC DESCRIPTION
21	SMAC	SMA Counter Overflow Messages
22	SMAO	SMA Operational Syndromes
23	SMAS	SMA Software Syndromes
24	SMAH	SMA Hardware Syndromes
25	SMAT	SMA Hardware Syndromes - Trunks
26	SMAL	SMA Hardware Syndromes - Lines
27	SMAR	SMA Response Only Messages
28	RC	Recent Change Repeated Messages
29	IDSP	System Image Display Messages
30	MLG	Maintenance Logging Messages
31	RESP	Response Only Messages

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Table 4. Terminal Function Mnemonics.

TERMINAL FUNCTION	MNEMONIC	DESCRIPTION
0	Not used	Null
1	CMT1	Common Maintenance Terminal One
2	CMT2	Common Maintenance Terminal Two
3	RMT	Remote Maintenance Terminal
4	RAT	Remote Alarm Terminal
5	RTFT	Remote Traffic Facilities Terminal
6	RTAT	Remote Traffic Analysis Terminal
7	RNST	Remote Network and Switch Management Terminal
8	SOT	Service Order Terminal
9	RSOT	Remote Service Order Terminal
10	RLTT	Remote Line Test Terminal
11	TT0	Trunk Test Terminal Zero
12	TT1	Trunk Test Terminal One
13	TT2	Trunk Test Terminal Two
14	TT3	Trunk Test Terminal Three
15	TST	Trunk Supervisory Terminal
16	CCT	Call Charging Terminal

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Table 5. Routing Type Codes.

CODE	DESCRIPTION
RT0	All messages with RT0 are sent to Common Maintenance Terminal 1 (CMT1). There is no remote or alternate terminal; the command must specify a primary terminal function which is CMT1.
RT1	All messages are normally routed to the primary terminal. If the primary terminal goes out of service, the messages are diverted to the alternate terminal. The primary and alternate terminal functions must be specified.
RT2	All system-originated (S@) messages are routed to both the primary and alternate terminal functions. Response messages (R@) are routed similar to RT1. The primary and alternate terminal functions must be specified.
RT3	All messages (S@ and R@) are routed to both the primary and alternate terminal functions. The primary and alternate terminal functions must be specified.
RT4	If the night transfer is not in effect, all messages are routed to the primary terminal. If the night transfer is in effect, all messages are routed to the remote terminal. In either case, the messages are diverted to the alternate terminal if the primary or the remote terminal is out of service. The primary, alternate, and remote terminal functions must be specified.
RT5	All messages are routed to both the primary and remote terminals. The primary and remote terminal functions must be specified. NOTE: If the terminal functions must always be specified in the following order: primary, alternate (if any), and remote (if any).

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Table 6. Message Class Routing Types.

TERM ROUTE TYPE	SYSTEM-INITIATED MESSAGE		TEST-PERSONNEL-INITIATED MESSAGE	
	FIRST TERMINAL	SECOND TERMINAL	FIRST TERMINAL	SECOND TERMINAL
0	Primary only (must be CMT1)	No alternate	Originating Only (must be CMT1)	No alternate
1	Primary	Alternate (only if first terminal is out of service)	Originating	Alternate (only if first terminal is out of service)
2	Primary and Alternate		Originating	Alternate (only if first terminal is out of service)
3	Primary and alternate		Originating and alternate	
4	Primary or remote	Alternate (only if first terminal is out of service)	Originating or remote	Alternate (only if first terminal is out of service)
5	Primary and remote		Originating and remote	

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Table 7. Print Options.

PRINT OPTION	INFORMATION PRINTED
1	No information is printed if the diagnostic passes. If a failure occurs, the hardware identifier and the Some-Tests-Fail (STF) value is printed on the proper terminal. The printout is provided during system-initiated hardware routining only.
2	The STF value, the Diagnostic Fault Signature (DFS) value (in hexadecimal), and the Consistency Fail (CF) value (if applicable) are printed. Print option 2 is the default value for all diagnostics, except hardware routines. The purpose for this default value is to help achieve the system objective of minimizing printouts. If print option 2 is specified and either the All-Tests-Skipped (ATS) or Some-Tests-Skipped (STS) condition occurs, the respective message is included in the output.
3	The Diagnostic Data Buffer (DDB) (in hexadecimal), the STF value (in hexadecimal), and the CF value (if applicable) are printed. Only nonzero data words along with their word numbers are printed.
4	The same information is printed as in print option 3, except the data words are printed in binary.
5	If a single iteration is specified, the printout is the same as a print option 3. If multiple iterations are specified, the printout is the same as print option 3, except data for each individual iteration is printed as well as the combined iteration result.
6	The same information is printed as in print option 5, except the data words are in binary.
7	The Phase Fault Signature (PFS) (in hexadecimal), the DFS (in hexadecimal), and the STF value are printed. If the diagnostic is iterated, the CF values are printed.
8	The same information is printed as in print option 5, except that a PFS (in hexadecimal) is printed.

00372

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXX
      DFS XXXX XXXX
      STF XXXX XXXX
  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE PERMANENT TO INS.IDLE TROUBLE
```

Figure 1. Sample Option 1 Printout.

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXXX
      DFS XXXX XXXX
      STF XXXX XXXX
  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 2. Sample Option 2 Printout.

00373

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXX

  PHASE 00
     00:  0000 0001
     01:  0000 0001
     02:  0000 0001
     03:  0000 0001
     04:  0000 0001
     05:  0000 0001
     11:  000X XXXX (PATH INFORMATION - VARIABLE)

  PHASE 04
     01:  000X XXXX (SENSITIVITY VALUE - PATH INFORMATION)
       DFS XXXX XXXX
       STF 4800 0000
  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 3. Sample Option 3 Printout.

00374

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXX

  PHASE 00
        00:  0000 0000 0000 0000 0000 0000 0000 0001
        01:  0000 0000 0000 0000 0000 0000 0000 0001
        02:  0000 0000 0000 0000 0000 0000 0000 0001
        03:  0000 0000 0000 0000 0000 0000 0000 0001
        04:  0000 0000 0000 0000 0000 0000 0000 0001
        05:  0000 0000 0000 0000 0000 0000 0000 0001
        11:  0000 0000 0000 XXXX XXXX XXXX XXXX XXXX

  PHASE 04
        01:  0000 0000 0000 XXXX XXXX XXXX XXXX XXXX
          DFS XXXX XXXX
          STF 4800 0000

  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 4. Sample Option 4 Printout.

00375

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXX

  PHASE 00
        00:  0000 0001
        01:  0000 0001
        02:  0000 0001
        03:  0000 0001
        04:  0000 0001
        05:  0000 0001
        11:  000X XXXX

  PHASE 04
        01:  000X XXXX
          DFS XXXX XXXX
          STF 4800 0000

  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 5. Sample Option 5 Printout.

00376

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  ON ATTACHED XXX-XXXX

  PHASE 00
     ITER 1 OF 3
     00:  0000 0001
     01:  0000 0001
     02:  0000 0001
     03:  0000 0001
     04:  0000 0001
     05:  0000 0001
     11:  000X XXXX

     ITER 2 OF 3
     SAME AS PREVIOUS DATA

     ITER 3 OF 3
     SAME AS PREVIOUS DATA

     COMBINED ITER DATA
     SAME AS ITER DATA

  PHASE 04
      ITER 1 OF 3
      01:  000X XXXX

      ITER 2 OF 3
      SAME AS PREVIOUS DATA

      ITER 3 OF 3
      SAME AS PREVIOUS DATA

      COMBINED ITER DATA
      SAME AS ITER DATA

      DFS XXXX XXXX
       CF XXXX XXXX
      STF 4800 0000

  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 6. Sample Option 5 ITER 3 Printout.

00377

```
OK
JOB:XXXX
R@XXXX JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXX

  PHASE 00
        00:  0000 0000 0000 0000 0000 0000 0000 0001
        01:  0000 0000 0000 0000 0000 0000 0000 0001
        02:  0000 0000 0000 0000 0000 0000 0000 0001
        03:  0000 0000 0000 0000 0000 0000 0000 0001
        04:  0000 0000 0000 0000 0000 0000 0000 0001
        05:  0000 0000 0000 0000 0000 0000 0000 0001
        11:  0000 0000 0000 XXXX XXXX XXXX XXXX XXXX

  PHASE 04
        01:  0000 0000 0000 XXXX XXXX XXXX XXXX XXXX
     DFS XXXX XXXX
     STF 4800 0000

  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 7. Sample Option 6 Printout.

```
OK
JOB:XXXX
R@XXXX  JOB:XXXX
  DIAG RESULTS LINE 0.0.0.0.0.0.0
  DN ATTACHED XXX-XXXX

  PHASE 00
        00:  0000 0001
        01:  0000 0001
        02:  0000 0001
        03:  0000 0001
        04:  0000 0001
        05:  0000 0001
        11:  000X XXXX
       PFS   XXXX XXXX

  PHASE 01 ATP
  PHASE 02 ATP
  PHASE 03 ATP

  PHASE 04
        01:  000X XXXX
        PFS XXXX XXXX
        DFS XXXX XXXX
        STF 4800 0000

  STATUS CHANGE LINE 0.0.0.0.0.0.0
  INS.IDLE TROUBLE TO INS.IDLE TROUBLE
```

Figure 8. Sample Option 8 Printout.

00379

TYPE 2B PROCESSOR COMPLEX SYSTEM INITIALIZATION INSTALLATION TEST PROCEDURE

CONTENTS

1. GENERAL

2. PREREQUISITES

3. TEST OBJECTIVE

4. TEST PROCEDURE

LIST OF TABLES

Table 1. Test Procedure Steps That Effect Each Level of Initialization.

Table 2. Test Procedure.

LIST OF FIGURES

Figure 1. Sample CMC Status Dump.

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1. GENERAL

1.01 This section provides the installation test procedure for testing each level of initialization of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the system configuration is in the full duplex mode before performing the test procedure in this section.

2.03 Test personnel should have access to the following:

(a) Input/Output Message Manual (IOMM) for the system being installed.

(b) JD-XXXXX-OCD, Office (Site) Configuration Drawing.

(c) A Common Maintenance Terminal (CMT) is available for maintenance inputs.

(d) Four test telephones (designated A, B, C, and D) with working directory numbers for placing test calls.

(e) Section 227-200-105, Processor Control and Display Console - Description and Use.

(f) Section 227-200-104, Miscellaneous Status and Alarm Frame - Description and Use.

3. TEST OBJECTIVE

3.01 The objective of the test procedure in this section is to verify the manual interrupt function and initialization levels of the Type 2B Processor Complex.

4. TEST PROCEDURE

4.01 Table 1 indicates the steps in the procedure at which the initialization levels are effected and summarizes the effects on the system at each level. Sequentially perform the steps listed in Table 2 to verify the manual interrupt function and the various initialization levels. Figure 1 shows a sample Control and Memory Complex (CMC) status dump.

4.02 If an audible alarm sounds during testing, depress the AUDIBLE ALARM RESET pushbutton on the SYSTEM STATUS AND ALARM subpanel of the Status and Alarm Panel (SAP) located in the Miscellaneous Status and Alarm Frame (MSAF). This action silences the alarm and causes any SYSTEM ALARM lamp in the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark.

00382

Table 1. Test Procedure Steps That Effect Each Level of Initialization.

GROUP OF STEPS	LEVEL	EFFECT ON SYSTEM
1 through 5	Preconditioning	None.
6 through 10	Processor Control and Display Console (PCDC) (manual) interrupt; level 0 initialization	None.
11 through 16	Level 1 initialization	Maintenance activity is canceled and diagnostics are scheduled.
17 through 24	Level 2 initialization	Level 1 effects, plus loss of dial tone and calls that are in process of completion (i.e., being dialed).
25 through 29	Level 3 initialization	Levels 1 and 2 effects, plus loss of established calls.
30 and 31	Level 4 initialization	Levels 1, 2, and 3 effects.

00383

Table 2. Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Ensure that the system is in the full duplex mode.	
2	Input DUMP DATE	The terminal outputs the actual calendar date and day of the week (i.e., 06/07/78 MON).
3	Establish communication between the CDF and the SAP via the SWMN LINE jacks on the SAP.	
4	Place a local call from test telephone A to test telephone B and remain off-hook with test telephones A and B.	Conversation is possible between telephones A and B.
5	Momentarily place test telephone C off-hook. Wait for the result; then place test telephone C on-hook.	Dial tone is heard.
6	Input DUMP STAT CMC	The terminal outputs a printout that is similar to the one shown in Figure 1.
7	On the PCDC, depress the ENTRY START pushbutton and enter 0 on the keypad.	On the PCDC, the ENTRY START pushbutton lights and 0 is displayed.

00384

Table 2. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
8	Input DUMP STAT CMC Prior to completion of the printout, simultaneously depress the FORCE XCUTE and INIT pushbuttons on the PCDC.	On the PCDC, the ENTRY START pushbutton goes dark and PROGRAM CHECK is displayed. The terminal outputs a CMC status dump. (See Figure 1 for an example.)
9	Verify that the call from test telephone A to test telephone B is still established.	Conversation is still possible.
10	Momentarily place test telephone C off-hook. Wait for the result; then place test telephone C on-hook.	Dial tone is heard.
11	On the PCDC, depress the ENTRY START push-button and enter 1 on the keypad.	On the PCDC, the ENTRY START pushbutton lights and 1 is displayed.
12	Input DUMP STAT CMC Before completion of the printout, simultaneously depress the FORCE XCUTE and INIT pushbuttons on the PCDC.	The terminal stops printing the CMC status dump. On the PCDC, the following occur: (a) The INIT lamp momentarily lights. (b) The ENTRY START pushbutton goes dark. (c) PROGRAM CHECK is displayed.

Table 2. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
13	Input DUMP DATE	The terminal outputs the actual calendar date and day of the week.
14	Input DUMP TIME	The terminal outputs the actual time.
15	Verify that the call from test telephone A to test telephone B is still established.	Conversation is still possible.
16	Momentarily place test telephone C off-hook. Wait for the result; then place test telephone C on-hook.	Dial tone is heard.
17	On the PCDC, depress the ENTRY START pushbutton and enter 2 on the keypad.	On the PCDC, the ENTRY START pushbutton lights and 2 is displayed.
18	Place a local call from test telephone C to test telephone D. After the result occurs, place test telephones C and D on-hook. NOTE: Steps 19 through 23 must be performed within 45 seconds.	Ringback tone and ringing are heard.

00386

Table 2. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
19	From test telephone C, dial the first four digits of test telephone D.	
20	On the PCDC, simultaneously depress the FORCE XCUTE and INIT pushbuttons.	On the PCDC, the following occur: (a) The INIT lamp lights. (b) The ENTRY START lamp goes dark. (c) PROGRAM CHECK is displayed.
21	From test telephone C, complete dialing of the remaining three digits of test telephone D.	Ringback tone and ringing are not heard.
22	Momentarily place test telephone C on-hook. Then place test telephone C off-hook.	
23	Verify that the call from test telephone A to test telephone B is still established.	Conversation is still possible. About 50 seconds after step 20 is initiated, the following occur: (a) On the PCDC, the INIT lamp goes dark. (b) Dial tone is heard on test telephone C. (c) The terminal outputs a printout that indicates that the level 2 initialization is completed.
24	Verify that the time and date printed out in step 23 are current.	The printed time and date correspond to the actual time and date.

00387

Table 2. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
25	On the PCDC, depress the ENTRY START pushbutton and enter 3 on the keypad.	On the PCDC, the ENTRY START pushbutton lights and 3 is displayed.
26	On the PCDC, ~~simultaneously~~ simult- aneously depress the FORCE XCUTE and INIT pushbuttons.	On the PCDC, the following occur: (a) The INIT lamp lights. (b) The program check is reissued. (c) The ENTRY START lamp goes dark. An audible indication in the Network Units (NU's) indicates that the Magnetic Latching Reed (MLR) capsules are resetting.
27	Verify that conversation is not possible between test telephones A and B.	Conversation is not possible. About 50 seconds after performing step 26, the following occur: (a) On the PCDC, the INIT lamp goes dark. (b) The terminal outputs a printout that indicates that the level 3 initialization is completed.
28	Verify that the time and date printed out in step 27 are current.	The printed time and date correspond to actual time and date.
29	Re-establish a talk path between test telephones A and B.	Conversation is possible.

00388

Table 2. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
30	On the PCDC, depress the ENTRY START pushbutton and enter 4 on the keypad.	On the PCDC, the ENTRY START pushbutton lights and 4 is displayed.
31	Repeat steps 25 through 27.	The results correspond to the results in steps 25 through 27.

00389

```
I@1906 DUMP STATUS CMC OK
  JOB:0013

R@1906 JOB:0013 STATUS DUMP
   CP0 INS
   CP1 INS
   CP2 INS
   BUS0 INS
   BUS1 INS
   MU0.0.0 INS
   MU0.0.1 INS
   MU0.0.2 INS
   MU0.0.3 INS
   MU0.0.4 INS
   MU0.0.5 INS
   MU0.1.0 INS
   MU0.1.1 INS
   MU0.1.2 INS
   MU0.1.3 INS
   MU0.1.4 INS
   MU0.1.5 INS
   MU0.2.0 INS
   MU0.2.1 INS
   MU0.2.2 INS
   MU0.2.3 INS
   MU0.2.4 INS
   MU0.2.5 INS
   MU1.0.0 INS
   MU1.0.1 INS
   MU1.0.2 INS
   MU1.0.3 INS
   MU1.0.4 INS
   MU1.0.5 INS
   MU1.1.0 INS
   MU1.1.1 INS
   MU1.1.2 INS
   MU1.1.3 INS
   MU1.1.4 INS
   MU1.1.5 INS
   MU1.2.0 INS
   MU1.2.1 INS
   MU1.2.2 INS
   MU1.2.3 INS
   MU1.2.4 INS
   MU1.2.5 INS
```

Figure 1. Sample CMC Status Dump.

00390

```
PC0.0 INS.ACT
PC1.0 INS.SBY
MIU0.0 INS
MIU0.1 INS
MIU0.2 INS
MIU1.0 INS
MIU1.1 INS
MIU1.2 INS
PIU0 INS
PIU1 INS
PCDC INS
CM0 INS
CM1 INS
RM0 INS
RM1 INS
PCLK0 INS.ACT
PCLK1 INS.SBY
CPPZ0 INS
CPPZ1 INS
CPPZ2 INS
MPZ0.0.0 INS
MPZ0.0.1 INS
MPZ0.1.0 INS
MPZ0.1.1 INS
MPZ0.2.0 INS
MPZ0.2.1 INS
MPZ1.0.0 INS
MPZ1.0.1 INS
MPZ1.1.0 INS
MPZ1.1.1 INS
MPZ1.2.0 INS
MPZ1.2.1 INS
PIPZ0.0 INS
PIPZ0.1 INS
PIPZ1.0 INS
PIPZ1.1 INS
```

Figure 1. Sample CMC Status Dump (Continued).

00391

TYPE 2B PROCESSOR COMPLEX
GENERIC AND CUSTOMER DATA BASE LOAD VERIFICATION
INSTALLATION TEST PROCEDURE

CONTENTS

1. GENERAL

2. PREREQUISITES

3. TEST OBJECTIVES

4. TEST PROCEDURE AND VERIFICATION

LIST OF TABLES

Table 1. Test Procedure

Table 2. Input Digit Description.

Table 3. Binary Weights of PUM's for the IOAF.

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1. GENERAL

1.01 This section provides the installation test procedure for loading and verifying the generic and customer (office-dependent or ODD) data base tapes for the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500IT).

2.02 The following equipment is required to perform the test procedure in this section:

(a) Common Maintenance Terminal (CMT).

(b) Generic load tape.

(c) Customer data base load tape.

(d) A reel of scratch tape.

2.03 Test personnel should have access to the following documentation:

(a) Module editor listing (FP-500000-GME).

(b) Generic program listing (FP-500000-GLF).

(c) Customer data base load program listing.

(d) Central processor unit equipment location job drawing (JD-XXXXX-CPEL).

(e) Section 227-200-105, Processor Control and Display Console - Description and Operation.

00393

2.04 Ensure that the following conditions exist prior to performing the loading procedure:

(a) The correct cards are installed in the memory complex.

(b) A successful X-ray has been accomplished on all copies of the Central Processor (CP), memory complex, Peripheral Controller (PC), at least one Input/Output Access Frame (IOAF) and Magnetic Tape Unit (MTU), and all peripheral matrices and interfaces.

3. TEST OBJECTIVES

3.01 The objectives of the test procedure in this section are to load and verify the generic and customer data base tapes.

4. TEST PROCEDURE AND VERIFICATION

4.01 Sequentially perform the steps in Table 1 to load and verify the generic and ODD tapes and to initialize the system, thereby completing the test procedure and leading to an idle system loop.

4.02 Tables 2 and 3 are referenced in Table 1. Table 2 defines the input digits used in the test procedure, and Table 3 gives the binary weights of the Peripheral Unit Matrices (PUM's) for the IOAF. This information is also referenced in Table 2.

4.03 After completion of system initialization, the CMT will print a message indicating that the level of initialization entered was completed, along with other system messages.

4.04 If any operation fails to produce the indicated result/system response, correct the fault, entering any necessary patches via a MEMORY MODIFY command.

4.05 Dump a tape containing the merged generic and ODD tapes and any inserted patches. This will eliminate the need to reload two tapes and re-enter the patches if a system reload is required.

4.06 The system is now in an idle condition and normal testing can begin. Patches that may have been inserted to obtain an idle condition should be evaluated as testing progresses to determine whether or not they are still required.

Table 1. Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Mount the generic load tape on the X-ray MTU.	
2	On the MTU, depress the LOAD and ON LINE pushbuttons.	On the MTU, the LOAD and ON LINE lamps light.
3	On the PCDC, depress the CLEAR and ENTRY START pushbuttons.	On the PCDC, the ENTRY START pushbutton lights.
4	On the PCDC keypad, enter aaaaaaa. where aaaaaaa = an input word as defined in Table 2 and 3.	On the PCDC, aaaaaaa is displayed.
5	On the PCDC, simultaneously depress the FORCE XCUTE pushbutton and one of the MASTER STATUS CP pushbuttons.	On the PCDC, the FORCE XCUTE pushbutton lights. On the MTU, the tape starts to move and memory loading begins.
6	On the PCDC, depress the ENTRY START pushbutton.	On the PCDC, the ENTRY START pushbutton goes dark.
7.	Repeat step 5.	On the PCDC, the following occur: (a) The FORCE XCUTE pushbutton goes dark. (b) When loading of memory is complete, TAPE IS LOADED is displayed.
8	Remove the generic tape and mount the ODD tape on the MTU. (If desired, the ODD tape may be mounted on a different MTU with different loader parameters.)	
9	Repeat steps 2 through 4.	The results correspond to those in steps 2 through 4.

Table 1. Test Procedure (continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
10	On the PCDC, depress the DATA FCN pushbutton.	On the MTU, the tape starts to move and memory loading begins. When loading of memory is complete, TAPE IS LOADED is displayed.
11	Remove the ODD tape and mount a scratch tape.	
12	On the PCDC, depress the ENTRY START pushbutton and enter 4 on the keypad.	On the PCDC, the ENTRY START pushbutton lights and 4 is displayed.
13	On the PCDC, simultaneously depress the FORCE XCUTE and INITIALIZATION pushbuttons.	During initialization, any lit alarm lamps go dark. On the PCDC, the following occur: (a) The FORCE XCUTE pushbutton momentarily lights. (b) The ENTRY START pushbutton goes dark. (c) When initialization is complete, the prime time and total time used by the system are displayed. NOTE: At this point, the system is fully operational.

Table 2. Input Digit Description.

DIGIT NO.	DESCRIPTION
1	Indicates the bus that is to be loaded where 0 = bus 0 1 = bus 1 2 = both bus 0 and bus 1
2	Indicates the Peripheral Interface Unit (PIU) that is to be used for loading where 0 = PIUØ 1 = PIU1
3	Indicates the location of ISØ where 0 = PUØ.Ø.Ø 1 = MU1.Ø.Ø 2 = MU* Ø.Ø (* = both MUØ and MU1)
4	Indicates the PC number for the IOAF.
5 and 6	Indicates the matrix number for the IOAF. (Refer to Table 3.)
7	Indicates the routine, load, and bypass indicators where 0 = routine only 1 = load into current map only 3 = load into current map and bypass read-after-write check 5 = load into current map and bypass tape errors 7 = load into current map and bypass read-after-write check and tape errors 9 = load into Fixed Office-Dependent (FOD) map only B = load into FOD map and bypass read-after-write check D = load into FOD map and bypass tape errors F = load into FOD map and bypass read-after-write check and tape errors

Table 2. Input Digit Description (continued).

DIGIT NO.	DESCRIPTION
8 (optional)	Indicates the update tape indicator where 0 = no update records on tape 1 = update forward mode with no override 5 = update reverse mode with no override 3 = update forward mode and override old data 7 = update reverse mode and override old data

Table 3. Binary Weights of PUM's for the IOAF.

PUM NO.	INPUT DIGIT	
	DIGIT 4 PERIPHERAL CONTROLLER NO.	DIGITS 5 AND 6 MATRIX NO.
00.02	0	02
00.03	0	03
00.04	0	04
00.05	0	05
00.06	0	06
00.07	0	07
00.08	0	08
00.09	0	09
00.10	0	10
00.11	0	11
00.12	0	12
00.13	0	13
00.14	0	14
00.15	0	15
00.18	0	18
00.19	0	19
00.20	0	20
00.21	0	21
00.22	0	22
00.23	0	23
00.24	0	24
00.25	0	25
00.26	0	26
00.27	0	27
00.28	0	28
00.29	0	29
00.30	0	30
00.31	0	31

TYPE 2B PROCESSOR COMPLEX
MAGNETIC TAPE UNIT STATUS
INSTALLATION TEST PROCEDURE

CONTENTS

1. GENERAL

2. PREREQUISITES

3. TEST OBJECTIVE

4. TEST PROCEDURE

LIST OF TABLES

Table 1. Test Procedure.

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00401

1. GENERAL

1.01 This section provides the installation test procedure for testing allowed and denied status transition controls and indications for the Magnetic Tape Units (MTU's) of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic No. 2 EAX, refer to Section 222-000-500; for an international No. 2 EAX, refer to Section 229-001-500IT).

2.02 Ensure that the following conditions exist before performing the test procedure in this section:

(a) All Type 2B Processor Complex units are free of known faults and are capable of being placed in service.

(b) All lamps and pushbuttons on the Processor Control and Display Console (PCDC) are in their normal or unoperated positions.

(c) All lamps on the SYSTEM STATUS AND ALARM subpanel of the Status and Alarm Panel (SAP) are unlit.

(d) One terminal is available for maintenance inputs.

(e) Section 227-202-501, Type 2B Processor Complex Control and Memory Complex - Installation Test Procedure, has been successfully completed.

(f) All non-billing equipped MTU's have scratch tapes with write-enable rings loaded and at the Beginning Of Tape (BOT) in the REMOTE mode. MTU0 is in the In-Service Active Billing (INS.ACT.BILLING) mode and will accept billing data from tape serial number 000002. MTU1 is in the In-Service Standby Billing (INS.SBY BILLING) mode and will not accept billing data from tape serial number 000003.

(g) Billing tapes 000004 through 000012 are available.

2.03 Test personnel should have access to the following documentation:

(a) An Input/Output Message Manual (IOMM) for the system being tested.

(b) EL-15012, Type 2B Processor Complex Input/Output Access Frame Circuit Drawing.

3. TEST OBJECTIVE

3.01 The objective of the test procedure in this section is to verify the allowed and denied status transitions of the MTU's.

4. TEST PROCEDURE

4.01 Sequentially perform the steps in Table 1 to test the status transitions of the MTU's.

4.02 Input all messages via a maintenance terminal.

4.03 If any step in this test procedure fails to produce the indicated result/system response, correct the problem and perform the test on that MTU again.

4.04 Each time an audible alarm sounds during testing, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the audible alarm and causes the appropriate SYSTEM ALARM lamp(s) on the SAP to go dark. Any PERIPHERAL ALARMS lamps that may have lit, will remain lit until the problem is corrected. If any subsequent system alarms should occur, the appropriate audible alarm will sound again and lamp(s) will light.

Table 1. Test Procedure.

STEP	OPERATION	RESULT
1	Input PUT INS MTUO BILL:000002,aaaa In this table aaaa = tape generation number	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTUO INS.ACT BILLING TO INS.ACT BILLING
2	Input FORCE INS MTUO BILL:000002,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTUO INS.ACT BILLING TO INS.ACT BILLING
3	Input PUT ACT MUTO BILL:000002,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU INS.ACT BILLING TO INS.ACT BILLING
4	Input FORCE ACT MTUO BILL:000002,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTUO INS.ACT BILLING TO INS.ACT BILLING

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
5	Input DIAG MTU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU0 INS.ACT BILLING TO INS.ACT BILLING
6	Input PUT INS MTU1 BILL:000003,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 INS.SBY BILLING TO INS.SBY BILLING
7	Input FORCE INS MTU1 BILL:000003,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 INS.SBY BILLING TO INS.SBY BILLING
8	Input DIAG MTU1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU1 ATP STATUS CHANGE MTU1 INS.SBY BILLING TO INS.SBY BILLING

00405

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
9	Input PUT OOS MTU1	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU INS.SBY BILLING TO OOS.MM MINOR ALARM
10	Input PUT OOS MTU1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 OOS.MM TO OOS.MM
11	Input FORCE OOS MTU1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 OOS.MM TO OOS.MM
12	Input PUT INS MTU1 BILL:000003,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR.

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU1 ATP STATUS CHANGE MTU1 OOS.MM TO INS.SBY BILLING
13	Input FORCE OOS MTU1	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.SBY BILLING TO OOS.MM MINOR ALARM
14	Input PUT ACT MTU1 BILL:000003,aaaa	On the SAP, the SYSTEM ALARM MINOR lamp lights: On the MTU under test, the following occur: (a) The MTU0 ACTIVE BILLING lamp goes dark. (b) The MTU0 LOAD lamp lights. (c) The MTU1 ACTIVE BILLING lamp lights. (d) The MTU1 LOAD lamp goes dark.

00407

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX S@XXXX BILLING TAPE TERMINATED MTU0 BLOCK COUNT IS 00000001 R@XXXX JOB:XXXX DIAG RESULTS MTU1 ATP STATUS CHANGE MTU1 OOS.MM TO INS.ACT.BILLING S@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT BILLING TO OOS.SYS MINOR ALARM
15	Input PUT OOS MTU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU0 OOS.SYS TO OOS.MM
16	Load tape 000004 on MTU0.	
17	Input FORCE ACT MTU0 BILL:000004,aaaa	On the SAP, the SYSTEM ALARM MINOR lamp lights. On the MTU, the following occur: (a) The MTU0 ACTIVE BILLING lamp lights. (b) The MTU0 LOAD lamp goes dark. (c) The MTU1 ACTIVE BILLING lamp goes dark. (d) The MTU1 LOAD lamp lights.

00408

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX S@XXXX BILLING TAPE TERMINATED MTU1 BLOCK COUNT IS 00000001 R@XXXX JOB:XXXX STATUS CHANGE MTU0 OOS.MM TO INS.ACT.BILLING S@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.ACT.BILLING TO OOS.SYS MINOR ALARM
18	Load tape 000005 on MTU1.	
19	Input PUT ACT MTU1 BILL:000005,aaaa	On the SAP, the SYSTEM ALARM MINOR lamp lights. On the MTU the following occur: (a) The MTU0 ACTIVE BILLING lamp goes dark. (b) The MTU0 LOAD lamp lights. (c) The MTU1 ACTIVE BILLING lamp lights. (d) The MTU1 LOAD lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU1 ATP STATUS CHANGE MTU1 OOS.SYS TO INS.ACT.BILLING

00409

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		S@XXXX BILLING TAPE TERMINATED MTU0 BLOCK COUNT IS 00000001 S@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.BILLING TO OOS.SYS MINOR ALARM
20	Load tape 000006 on MTU0.	
21	Input PUT INS MTU0 BILL:000006,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 OOS.SYS TO INS.SBY.BILLING
22	Input PUT ACT MTU0 BILL:000006,aaaa	On the SAP, the following lamps light: (a) SYSTEM ALARM MINOR. (b) PERIPHERAL EQUIPMENT MINOR. (c) MTU MINOR. On the MTU, the following occur: (a) The MTU0 ACTIVE BILLING lamp lights. (b) The MTU0 LOAD lamp goes dark. (c) The MTU1 ACTIVE BILLING lamp goes dark. (d) The MTU1 LOAD lamp lights.

00410

Table 1. Test Procedure (Continued).

STEP		OPERATION	RESULT
			The terminal outputs OK JOB:XXXX S@XXXX BILLING TAPE TERMINATED MTU1 BLOCK COUNT IS 00000001 R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 INS.SBY.BILLING TO INS.ACT.BILLING S@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.ACT.BILLING TO OOS.SYS MINOR ALARM
23		Load tape 000007 on MTU1.	
24		Input FORCE INS MTU1 BILL:000007,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 OOS.SYS TO INS.SBY.BILLING
25		Input FORCE ACT MTU1 BILL:000007,aaaa	On the SAP, the following lamps light: (a) SYSTEM ALARM MINOR. (b) PERIPHERAL EQUIPMENT MINOR. (c) MTU MINOR.

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		On the MTU, the following occur: (a) The MTU0 ACTIVE BILLING lamp goes dark. (b) The MTU0 LOAD lamp lights. (c) The MTU1 ACTIVE BILLING lamp lights. (d) The MTU1 LOAD lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.SBY.BILLING TO INS.ACT.BILLING S@XXXX BILLING TAPE TERMINATED MTU0 BLOCK COUNT IS 00000001 S@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.BILLING TO OOS.SYS MINOR ALARM
26	Load tape 000008 on MTU0.	
27	Input FORCE ACT MTU0 BILL:000008,aaaa	On the SAP, the SYSTEM ALARM MINOR lamp lights. On the MTU, the following occur: (a) The MTU0 ACTIVE BILLING lamp lights. (b) The MTU0 LOAD lamp goes dark. (c) The MTU1 ACTIVE BILLING lamp goes dark. (d) The MTU1 LOAD lamp lights.

00412

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX S@XXXX BILLING TAPE TERMINATED MTU1 BLOCK COUNT IS 00000001 R@XXXX JOB:XXXX STATUS CHANGE MTU0 OOS.SYS TO INS.ACT.BILLING S@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.ACT.BILLING TO OOS.SYS MINOR ALARM STATUS CHANGE MTU0 OOS.SYS TO INS.ACT.BILLING STATUS CHANGE MTU1 INS.ACT.BILLING TO OOS.SYS MINOR ALARM
28	Input FORCE OOS MTU1	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 OOS.SYS TO OOS.MM
29	Load tape 000009 on MTU1.	
30	Input FORCE INS MTU1 BILL:000009,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR.

00413

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 OOS.MM TO INS.SBY.BILLING
31	Input FORCE ACT MTU1 BILL:000009,aaaa	On the SAP, the following lamps light: (a) SYSTEM ALARM MINOR. (b) PERIPHERAL EQUIPMENT MINOR. (c) MTU MINOR. On the MTU, the following occur: (a) The MTU0 ACTIVE BILLING lamp goes dark. (b) The MTU0 LOAD lamp lights. (c) The MTU1 ACTIVE BILLING lamp lights. (d) The MTU1 LOAD lamp goes dark. The terminal outputs OK JOB:XXXX S@XXXX BILLING TAPE TERMINATED MTU0 BLOCK COUNT IS 00000001 R@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.SBY.BILLING TO INS.ACT.BILLING S@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.BILLING TO OOS.SYS MINOR ALARM

00414

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
32	Input DIAG MTU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS RESULTS MTU0 OOS.MM TO OOS.MM
33	Load tape 000010 on MTU0.	
34	Input PUT INS MTU0 BILL:000010,aaaa	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 OOS.MM TO INS.SBY.BILLING
35	Input FORCE OOS MTU1	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. On the MTU, the following occur: (a) The MTU1 ACTIVE BILLING lamp goes dark. (b) The MTU0 ACTIVE BILLING lamp lights.

00415

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 INS.ACT.BILLING TO OOS.MM MINOR ALARM S@XXXX BILLING TAPE TERMINATED MTU1 BLOCK COUNT IS 00000001 S@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.SBY.BILLING TO INS.ACT.BILLING STATUS CHANGE MTU0 INS.SBY.BILLING TO INS.ACT.BILLING MINOR ALARM
36	Input FORCE OOS MTU0	On the SAP, the following occur: (a) The PERIPHERAL EQUIPMENT MAJOR lamp lights. (b) The MTU MAJOR lamp lights. On the MTU, the following occur: (a) The MTU0 ACTIVE BILLING lamp goes dark. (b) The MTU1 LOAD lamp lights. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.BILLING TO OOS.MM MAJOR ALARM BILLING TAPE TERMINATED MTU0 BLOCK COUNT IS XXXXXXX

00416

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
37	Manually move the tape off the BOT, then input FORCE ACT MTU0 BILL:000010,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC033 TAPE NOT AT BOT STATUS CHANGE MTU0 OOS.MM TO OOS.MM .
38	Manually put MTU0 and MTU1 at the BOT.	
39	Load tape 000011 on MTU1.	
40	Input FORCE ACT MTU1 BILL:000011,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MAJOR. (b) MTU MAJOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU1 OOS.MM TO INS.ACT.BILLING
41	Input PUT ACT MTU1 MEMIN:000011,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 INS.ACT.BILLING TO INS.ACT.BILLING

00417

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
42	Input PUT ACT MTU1 MEMOUT:000011,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 INS.ACT.BILLING TO INS.ACT.BILLING
43	Input PUT ACT MTU1 DATA:000011,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU1 INS.ACT.BILLING TO INS.ACT.BILLING
44	Input PUT ACT MTU0 MEMIN:000011,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU0 OOS.MM TO INS.ACT.MEMIN
45	Input PUT ACT MTU0 MEMOUT:000011,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS TRANSITION STATUS CHANGE MTU0 INS.ACT.MEMIN TO INS.ACT.MEMIN

00418

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
46	Input PUT OOS MTU0	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX ~~DIAG RESULTS MTU0~~ ~~ATP~~ STATUS CHANGE MTU0 ~~005.MM TO~~ INS.ACT.MEMIN ~~INS.ACT.MEMOUT~~ TO 005.MM ~~MINOR~~ ALARM
47	Input PUT ACT MTU0 MEMOUT:000011,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 OOS.MM TO INS.ACT.~~DATA~~ MEMOUT
48	Input PUT ACT MTU0 DATA:000011,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC076 INVALID STATUS CHANGE STATUS CHANGE MTU0 INS.ACT.MEMOUT TO INS.ACT.MEMOUT

00419

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
49	Input PUT OOS MTU0	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.MEMOUT TO OOS.MM MINOR ALARM
50	Input PUT ACT MTU0 DATA:000011,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 OOS.MM TO INS.ACT.DATA
51	Input PUT OOS MTU0	On the SAP, the following lamps light: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR.

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT
		The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.DATA TO OOS.MM MINOR ALARM
52	Load tape 000012 on MTU0.	
53	Input PUT INS MTU0 BILL:000012,aaaa	On the SAP, the following lamps go dark: (a) PERIPHERAL EQUIPMENT MINOR. (b) MTU MINOR. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 OOS.MM TO INS.SBY.BILLING
54	If the office-dependent data base specifies, verify the volume label by inputting FORCE ACT MTU0 BILL:000011,aaaa	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX TC344 INVALID VOLUME LABEL STATUS CHANGE MTU0 INS.SBY.BILLING TO OOS.RCVY

00421

TYPE 2B PROCESSOR COMPLEX SYSTEM RECOVERY FEATURES INSTALLATION TEST PROCEDURE

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2. PREREQUISITES

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4. TEST PROCEDURE

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Table 1. Test Procedure.

LIST OF ILLUSTRATIONS

Figure 1. Typical CMC Recovery Report.

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00422

1. GENERAL

1.01 This section provides the procedure for testing the system recovery features of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 Ensure that the following conditions exist before performing the test procedure in Table 1:

(a) All Type 2B Processor Complex units are free of faults and are capable of being placed in service.

(b) The system configuration is in the full duplex mode.

(c) All switches and pushbuttons on the Status and Alarm Panel (SAP) of the Miscellaneous Status and Alarm Frame (MSAF) are in their normal or unoperated position.

(d) All lamps on the SYSTEM STATUS AND ALARM subpanel of the SAP and all lamps on the Processor Control and Display Console (PCDC) are unlit.

(e) A terminal is available for maintenance inputs and outputs.

(f) A level 4 initialization has been manually generated from the PCDC.

2.02 Test personnel should have access to the following documentation:

(a) An Input/Output Message Manual (IOMM) for the system being tested.

(b) The Office (Site) Configuration Drawing (JD-XXXXX-OCD) for the system being tested.

(C) EL-XXXXX circuit drawings for the Type 2B Processor Complex.

2.03 A reel of daisy-chain strapping wire is needed for inserting faults.

3. TEST OBJECTIVE

3.01 The objective of the test procedure in this section is to verify recovery features when a fault exists in one of the reconfigurable units (CP, BUS, RM, CM, MIU, MU, PIU, PC) of the Type 2B Processor Complex.

00423

4. TEST PROCEDURE

4.01 Sequentially perform the steps listed in Table 1 to test the recovery process. In this test procedure, the fault locations are given by frame type/number, frame file, file slot, and pin number. The term "momentarily" implies at least a 10-second interval. Refer to Figure 1 for a typical Type 2B Processor Complex recovery report.

4.02 Input all messages via a maintenance terminal.

4.03 If the operation of any step in Table 1 fails to produce the indicated result/system response, correct the problem and perform the test again.

4.04 Each time the audible alarm sounds, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the alarm and causes the appropriate SYSTEM ALARM lamp(s) on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark. Any PERIPHERAL ALARMS lamps that may have lit, will remain lit, until the problem is corrected. If any subsequent system alarms should occur, the appropriate audible alarm will sound again and lamp(s) will light.

00424

Table 1. Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Insert a fault in the logical unit by momentarily strapping backplane pin CPCF, H, 16, 69 frame file slot pin to backplane ground pin CPCF, H, 16, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the following lamps light: (a) CE MIN lamp. (b) OOS lamp for CP2. (c) MASTER STATUS CP0 lamp. The maintenance terminal outputs the following CMC RECOVERY message: S@XXXX JOB:XXXX DIAG RESULTS CP2 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE CP2 OOS.RCVY TO OOS.SYS MINOR ALARM
2	Input PUT INS.CP2	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the following lamps go dark: (a) CE MINOR lamp. (b) OOS lamp for CP2. (c) MASTER STATUS CP0 lamp. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CP2 ATP STATUS CHANGE CP2 OOS.SYS TO INS

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
3	Insert a fault in logical unit BUS1 by momentarily strapping backplane pin CPCF, H, 01, 93 to backplane ground pin CPCF, H, 01, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the CE MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS BUS1 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE BUS1 OOS RCVY TO OOS.SYS MINOR ALARM
4	Input PUT INS.BUS1	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the CE MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS BUS1 ATP STATUS CHANGE BUS1 OOS.SYS TO INS

00426

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
5	Insert a fault in logical unit RM1 by momentarily strapping backplane pin CPCF, G, 10, (64,66)* to backplane ground pin CPCF, G, 10, 51. * Strap these pins together, then ground.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the CE MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS RM1 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE RM1 OOS.RCVY TO OOS.SYS MINOR ALARM
6	Input PUT INS.RM1	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the CE MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS RM1 ATP STATUS CHANGE RM1 OOS.SYS TO INS

00427

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
7	Insert a fault in logical unit CMO by mementarily strapping backplane pin CPCF, TA, 9, 72 to backplane ground pin CPCF, TA, 9, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the CE MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS CMO DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE CMO OOS.RCVY TO OOS.SYS MINOR ALARM
8	Input PUT INS.CMO	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the CE MINOR lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS CMO ATP STATUS CHANGE CMO OOS.SYS TO INS

00428

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
9	Insert a fault in logical unit PCLK0 by mementarily strapping backplane pin CPCF, B, 17, 20 to backplane ground pin CPCF, B, 17, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the CLOCK MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS PCLK0 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE PCLK0 OOS.RCVY TO OOS.SYS MINOR ALARM
10	Input PUT INS.PCLK0	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the CLOCK MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PCLK0 ATP STATUS CHANGE PCLK0 OOS.SYS TO INS.SBY

00429

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
11	Insert a fault in logical unit PIU0 by mementarily strapping backplane pin CPCF, TA, 01, 67 to backplane ground pin CPCF, TA, 01, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the PERIF MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS PIU0 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE PIU0 OOS.RCVY TO OOS.SYS MINOR ALARM
12	Input PUT INS.PIU0	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the PERIF MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PIU0 ATP STATUS CHANGE PIU0 OOS.SYS TO INS

00430

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
13	Insert a fault in logical unit MIU0.0 by momentarily strapping backplane pin MEAF, TA, 35, 13 to backplane ground pin MEAF, TA, 35, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the MEMORY MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS MIU0.0 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE MIU0.0 OOS.RCVY TO OOS.SYS MINOR ALARM
14	Input PUT INS.MIU0.0	On the SAP, the CMC ALARM MINOR lamp goes dark. On the PCDC, the MEMORY MIN lamp goes dark. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MIU0.0 ATP STATUS CHANGE MIU0.0 OOS.SYS TO INS

00431

Table 1. Test Procedure (Continued).

STEP	OPERATION	RESULT/SYSTEM RESPONSE
15	Insert a fault in logical unit PC1.0 by momentarily strapping backplane pin NPCF001, TA, 33, 37 to backplane ground pin NPCF001, TA, 33, 51.	On the SAP, the following occur: (a) The SYSTEM ALARM MINOR lamp lights. (b) The CMC ALARM MINOR lamp lights. (c) The minor audible alarm sounds. On the PCDC, the PERIF MIN lamp lights. The terminal outputs the following CMC recovery message: S@XXXX JOB:XXXX DIAG RESULTS PC1.0 DFSXXXX XXXX CFXXXX XXXX STFXXXX XXXX STATUS CHANGE PC1.0 OOS.RCVY TO OOS.SYS MINOR ALARM
16	Input PUT INS.PC1.0	On the SAP, the following lamps go dark: (a) The SYSTEM ALARM MINOR lamp. (b) The CMC ALARM MINOR lamp. On the PCDC, the following lamps go dark: (a) PERIF MIN lamp. (b) The OOS lamp for PC1.0. The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS PC1.0 ATP STATUS CHANGE PC1.0 OOS.SYS TO INS

00432

```
S@0000
  CMC RECOVERY 00/00/00
  HARDWARE TYPE - 0012 INTERRUPT REFERENCING PU00006 IAR=DFBB8
  RETURN TO PTE  LEVEL 4 INITIALIZATION

  ASSEMBLED   000  111  111  000  000  0  000  000  000  000  000  0
     ERRORS:  000  000  000  000  000  1  000  000  000  000  000  0

  CURR:IND=BEB2  0500  CCW=11  00  00  11  00  00  00  11  11  01  1111  01  0001  01
  FIRM:IND=FEB4  0060  CCW=00  11  11  00  11  11  11  00  00  01  1111  01  1000  01
  ORIG:IND=DA30  0000  CCW=00  11  11  00  11  11  11  00  00  01  1111  01  1000  01

  SPR=8DD0  0000  GR1=FFFB  0009  GR2=0000  0003  GR3=0001  0000
  GR4=0000  0000  GR5=0000  0000  GR6=012C  0000  GR7=012C  F521  SAR=12C

  CIR=C388  0006  CDS=B240  B240  DTR=0000  0000  GLV=0000  0000  IBP=0000  0000
  NPS=8000  FBB3  PCS=C680  0006   CC=0012

  LAST 12 WORDS OF STACK FROM 000 TO 000
  0000  0000    0000  0000    0000  0000    0000  0000    0000  0000    0000  0000
  0000  0000    0000  0000    0000  0000    0000  0000    0000  0000    0000  0000

  END CMC RECOVERY
```

Figure 1. Typical CMC Recovery Report.

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TYPE 2B PROCESSOR COMPLEX MAGNETIC TAPE UNIT RECOVERY FEATURES INSTALLATION TEST PROCEDURE

1. GENERAL

1.01 This section provides the procedure for testing the Magnetic Tape Unit (MTU) recovery features of the Type 2B Processor Complex.

2. PREREQUISITES

2.01 For general prerequisites, refer to the field implementation plan for the system being installed (i.e., for a domestic-version No. 2 EAX, refer to Section 222-000-500; for an international-version No. 2 EAX, refer to Section 229-001-500 IT).

2.02 Ensure that the following conditions exist before performing the test in this section:

(a) All Type 2B Processor Complex units are free of all known faults and in service.
(b) The system configuration is in the duplex mode with all copies 0 in the primary mode.
(c) All lamps and pushbuttons on the Processor Control Display Console (PCDC) are in their normal or unoperated position.
(d) All lamps on the SYSTEM STATUS AND ALARM subpanel of the Status and Alarm Panel (SAP) except for the MTU alarm lamps are unlit.
(e) One terminal is available for maintenance inputs.
(f) All installation test procedures in the 227-203 subdivision of GTE Practices have been successfully completed.
(g) A level E2 initialization has been manually generated from the PCDC.
(h) A scratch tape with a write-enable ring has been loaded on the MTU to be tested and is at the beginning of the tape.
(i) All MTU's are in an out-of-service maintenance man (OOS.MM) status state.

2.03 Test personnel should have access to the following documentation:

(a) An Input/Output Message Manual (IOMM) for the system being tested.
(b) JD-XXXXX-OCD, Office (Site) Configuration Drawing.

2.04 A reel of daisy-chain strapping wire is needed for inserting faults.

3. TEST OBJECTIVE

3.01 The objective of the test in this section is to verify the ability of the system to recover from MTU faults.

4. TEST PROCEDURE

CAUTION: Exercise extreme caution when making the connections to the backplane during the test procedure. Incorrect backplane connections may cause hardware damage to the system.

4.01 Sequentially perform the steps listed in Table 1 to test the MTU recovery feature. Repeat this procedure for each equipped MTU. Table 2 lists the serial numbers, faults, and syndromes to be used in Table 1.

4.02 If the operation for any step in Table 1 fails to produce the indicated results, correct the problem and perform the test again.

4.03 Each time the audible alarm sounds, depress the AUDIBLE ALARM RESET pushbutton on the SAP. This action silences the alarm and causes any SYSTEM ALARM lamp on the SYSTEM STATUS AND ALARM subpanel of the SAP to go dark.

4.04 Input all messages via a maintenance terminal.

Table 1. Test Procedure.

STEP	OPERATION	RESULT/SYSTEM RESPONSE
1	Input PUT ACT MTU0 MEMOUT: 111111 where 111111 = the tape serial number	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX DIAG RESULTS MTU0 ATP STATUS CHANGE MTU0 OOS.MM TO INS.ACT.MEMOUT

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Table 1. Test Procedure (Continued).

2	Input WRITE TAPE IS: *PS:* where * = all implemented memory for that complex	The terminal outputs OK JOB:XXXX On MTU0, the tape starts moving.
3	Momentarily strap the A43-7 pin to the B29-87 pin on MTU0.	On the SAP, the PERIPHERAL EQUIPMENT MINOR, the SYSTEM ALARM MINOR, and PERIPHERAL ALARMS MTU MINOR lamps light. The terminal outputs R@XXXX JOB:XXXX WRITE TAPE TC012 HARDWARE NOT ACCESSABLE S@XXXX JOB:XXXX STATUS CHANGE MTU0 INS.ACT.MEMOUT TO OOS.RCVY MINOR ALARM
4	Input PUT OOS MTU0	The terminal outputs OK JOB:XXXX R@XXXX JOB:XXXX STATUS CHANGE MTU0 OOS.RCVY to OOS.MM MAJOR ALARM On the SAP, the PERIPHERAL EQUIPMENT MAJOR, the PERIPHERAL ALARMS MTU MAJOR, and the SYSTEM ALARM MAJOR lamps light.
5	Repeat steps 1 through 4 using the serial number and faults in Table 2.	Results correspond to steps 1 through 4 with the appropriate System Malfunction Analysis (SMA) hardware trace syndromes from Table 2 being printed.

Table 2. List of Serial Numbers, Faults, and Syndromes.

SERIAL NUMBER	FAULT STRAP A-43-7 CONNECTIONS	SMA HARDWARE TRACE SYNDROMES
111111	B-29-87 ($\overline{\text{TRDY}}$)	MTU: TRANSPORT NOT READY
222222	B-31-24 ($\overline{\text{DRA}}$)	MTU: FWD REW REV IN INCORRECT STATE
333333	B-31-73 ($\overline{\text{FBP}}$)	MTU: FWD REW REV IN INCORRECT STATE
444444	B-31-38 ($\overline{\text{LRCG}}$)	MTU: FWD REW REV IN INCORRECT STATE
555555	B-31-29 ($\overline{\text{VPCG}}$)	MTU: FWD REW REV IN INCORRECT STATE
666666	B-31-88 ($\overline{\text{CRCG}}$)	MTU: FWD REW REV IN INCORRECT STATE
777777	B-31-87 ($\overline{\text{BOPG}}$)	MTU: FWD REW REV IN INCORRECT STATE

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